Silicon Substrates With Buried Distributed Bragg Reflectors for Resonant Cavity-Enhanced Optoelectronics

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***Abstract*—We report on a commercially reproducible silicon wafer with a high-reflectance buried distributed Bragg reflector (DBR). The substrate consists of a two-period DBR fabricated using a double silicon-on-insulator (SOI) process. The buried DBR provides a 90% reflecting surface. We have fabricated resonant cavity-enhanced Si photodetectors with 40% quantum efficiency at 860 nm and a full-width at half-maximum of 29 ps suitable for 10 Gbps data communications. We have also implemented double-SOI substrates with 90% reflectivity covering 1300 and 1550 nm for use in Si-based optoelectronics.**

***Index Terms*—Distributed Bragg reflector, photodetector, resonant cavity enhanced, silicon, silicon-on-insulator.**

I. Introduction

MANY applications for optical micro resonators structures have emerged over the years, including light-emitting devices, modulators, and photodetectors, to name a few. The ever growing demand for high-speed optical communications has made resonant cavity-enhanced (RCE) photodetectors an important research topic over the last decade [1]. In semiconductors, such a resonant cavity can be formed using a buried reflector and the air/semiconductor top interface. The buried reflector is typically formed by alternating layers of semiconductors with different refractive indices. Due to the availability of heterostructures, compound semiconductors have been the focus of RCE photodetector development [1]. One of the many benefits of silicon, however, is the large index contrast provided by Si–SiO_2—nearly 60%, compared to 17% for GaAs–AlAs. This means that high reflectivity can be achieved with much fewer periods in a Si–SiO2 distributed Bragg reflector (DBR) as well as having a wider spectral stopband.

While there have been reports of multilayer silicon-on-insulator (SOI) wafers [2], to the authors' knowledge, there have been few efforts on purposely manufactured reflecting substrates. Ishikawa *et al.* [3], [4] used a combination of separation by implantation of oxygen (SIMOX) and epitaxy to develop a DBR with a peak reflectance of 90%. The DBR used five periods of Si–SiO_2, which were created using SIMOX to produce the buried oxide layer and molecular beam epitaxy (MBE) to grow the Si layers. The limitations related to the SIMOX process, as discussed below, required not only a complex fabrication process but also many layers to achieve the desired reflectivity.

We have introduced a commercially reproducible Si wafer with a high reflectance buried DBR for Si RCE optoelectronics [5]. These wafers, fabricated by a repeated SOI process, have buried DBR structures with reflectivity in excess of 90% using only a two-period Si–SiO_2 structure and have an epitaxy ready single crystalline surface. We report on the optical and electrical properties of the double-SOI wafers and present results on high-speed, high-efficiency RCE photodetectors fabricated on these reflecting Si substrates.

The inherent benefit of the RCE structure is to increase the bandwidth-efficiency product over a conventional photodetector. The quantum efficiency η of conventional detectors is governed by the optical absorption of the semiconductor material. For semiconductors with low absorption coefficients, thick absorption regions are required to achieve high η, limiting the bandwidth of photodetectors. Silicon-based photodetectors for applications in optical communications in the near-IR wavelength range between 800–900 nm suffer from low bandwidth-efficiency products due to the long absorption length necessitated by the small absorption coefficient. Increasing the bandwidth-efficiency product is the inherent benefit of an RCE structure, which relies on the constructive interference of a Fabry–Perot cavity to enhance the optical field inside the photodetector at specific wavelengths.

Numerous attempts have been made to fabricate Si RCE photodetectors [6]. Earlier devices utilized Si device structures deposited on top of dielectric mirrors. Various attempts included chemical vapor deposition (CVD) as well as molecular beam epitaxy (MBE) [7], which resulted in a polycrystalline Si device layer. Photodiodes fabricated on this device layer typically suffered from high dark currents. Schaub *et al.* [8] has reported Si RCE photodiodes with low dark currents that achieved a bandwidth in excess of 34 GHz—the highest speed recorded for Si p-i-n photodiodes. These RCE structures used a merged epitaxial layer overgrowth (MELO) process to form the absorption region on top of the buried DBR. Although this growth process is not a commercially viable technique, the results in themselves

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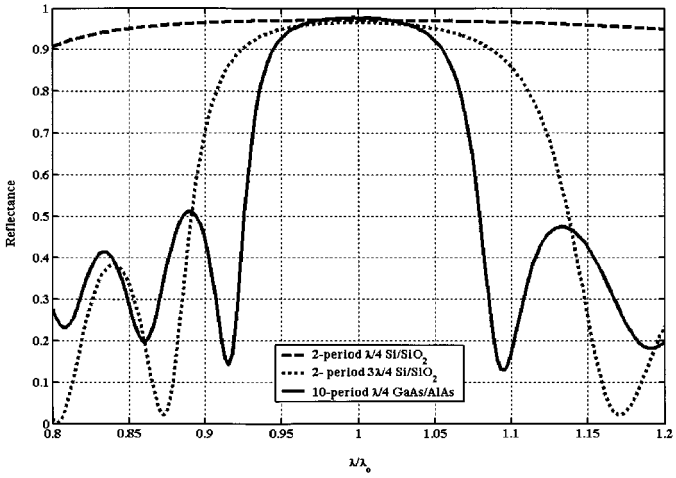

Fig. 1. Simulated reflectivity of $1/4\lambda$ and $3/4\lambda$ Si–SiO_2 two-period DBR as compared with a $1/4\lambda$ GaAs–AlAs 10-period DBR.

are significant; Schaub has shown that use of RCE for Si photodiodes can lead to significant leaps in device performance. With our double-SOI reflecting substrates, not only can RCE Si photodetectors be a commercial reality but also, due to the ubiquitous nature of the silicon industry, a wide array of other applications, such as wavelength sensors, RCE photodetector arrays, as well as on chip signal conditioning, become possible.

II. Optical Design Considerations

A typical DBR mirror is formed by alternating layers of $1/4\lambda$-thick dielectrics with different refractive indexes. The magnitude of the index contrast of the dielectric constituents determines the spectral width of the stopband, as well as the number of periods required for optimum reflectivity. Limitations in fabrication process, however, may not allow for layer thicknesses as thin as $1/4\lambda$, in which case one can also use $3/4\lambda$ layers. This will sacrifice the stopband width, but when using large index contrast dielectrics, the degradation is not problematic. For compound semiconductors, nearly lattice-matched GaAs–AlAs structures have been the most commonly used materials for DBRs, providing an index contrast of 17%. Si–SiO_2, on the other hand, with an index contrast of 60% can be used to make over 90% reflective DBRs with only two periods compared to 10 periods for GaAs–AlAs. Also, due to the larger index contrast, the stopband is significantly larger for both $1/4\lambda$ and $3/4\lambda$, two-period, Si–SiO_2 DBRs compared with the 10-period GaAs–AlAs structure. A comparison of the reflectivity of these DBRs can be seen in Fig. 1. Due to limitations in the wafer-fabrication process, we chose $3/4\lambda$ layer thicknesses for the DBR.

Previous attempts to develop Si–SiO_2 DBRs by Ishikawa *et al.* [3], [4] used a combination of SIMOX to produce the buried oxide layer and MBE to grow the Si layers. Their work showed that the choice of layer thickness for SiO_2 and Si was limited to a SiO_2–Si thickness ratio of less than unity due to poor interface morphology. This result is a critical limitation; as in an optimally tuned structure, the optical path lengths in SiO_2 and Si are identical, which means the layer thickness of SiO_2 is larger than that of Si since SiO_2 has a smaller refractive index. This means that the SiO_2–Si width ratio is greater than unity for an optimally tuned structure. They were able to produce highly reflective dielectric mirrors only after ten layers were grown. Another drawback of their technique is that it utilized a complex *in situ* implantation and epitaxy process that required specialized equipment. In contrast, we have developed a technique to fabricate optimized Si–SiO_2 DBRs using a commercially available SOI process.

III. Silicon on Insulator Background

The relentless drive of the silicon industry to produce high-speed circuits has resulted in numerous studies in the pursuit of advanced processing techniques. One of the techniques nurtured by these efforts has been SOI technology [9]. First investigated in the mid-1960s with the use of silicon-on-sapphire (SOS), SOI offered the hope of reduced device capacitances as well as the increased radiation hardness of silicon circuits. SOI wafers consist of a Si handle wafer, a buried oxide, and a single crystalline Si device layer (commonly referred to as the SOI layer). The increased cost of wafer fabrication and the relatively poor quality of the SOI device layer prevented the field from much advancement. Recently, as device speeds and the demand for low-voltage circuits have increased, there has been a resurgence of the SOI field. Currently, there are three major techniques for SOI manufacturing which include SIMOX, bonded and etched-back SOI (BESOI), and ion-cut.

A. SIMOX

SIMOX processing was first developed in 1966 as a means to replace SOS [10]. The process involves the implantation of a large dose of oxygen into a Si wafer. The wafer is then annealed at high temperature to enhance ripening of the implant and to form SiO_2. Due to the large concentration of oxygen in stoichiometric SiO_2, large doses of oxygen have to be implanted. Early problems inherent in the SIMOX process were large defect densities in the SOI layer due to implantation damage from the high energies and large implant doses. The high-dose implant of oxygen in Si causes threading defects (TD), which can be detrimental to device performance [11]. A major drawback to SIMOX is the depth limitation of the oxygen implant which correspondingly limits the thickness of the SOI layer (<0.3 μm). At the time this study was undertaken, the limited availability of deep oxygen implants as well as high defect densities eliminated SIMOX as a viable candidate for fabricating reflecting substrates. Current advancements have reduced TD density to acceptable levels [12], but SIMOX still requires an epitaxial layer to be grown and second SIMOX step, which is not offered by any commercial vendors.

B. BESOI

BESOI is the process of bonding two oxidized wafers and then etching back one of the wafer surfaces to yield a thin SOI layer [13]. The advantage of this method over SIMOX is the possibility of much larger top Si layer thickness. The key to BESOI is the availability of a highly selective etch stop in the sacrificial wafer. These etch stops can come in a variety of forms, the most popular being a highly doped boron [14] region or porous

Si [15]. Poor etch stop selectivity results in a highly nonuniform SOI layer that is unacceptable for device grade electronics. The first step in BESOI is to bring the wafers into contact at room temperature to form a bond via Van der Waals forces. The contacted wafers are then heated to strengthen the interface bonds. Next, the wafer is etched back, usually by a chemical reactant that consumes the top bulk Si layer up to the desired etch-stop, leaving a thin Si layer. A major problem inherent in the BESOI process is the relative inaccuracy in the etch-back process. Due to the uniformity problems of a chemomechanical etch, the Si device layer thickness is limited to greater than 0.3 μm [13]. This limitation precluded BESOI as being a viable candidate for making reflective substrates, although recent advancements have shown that Si layers as thin as 27 nm with thickness uniformity less than $\pm 5\%$ can be achieved [16].

C. Ion-Cut

The mechanism behind ion-cut is the blistering of Si [17]. Blistering, or flaking, is induced when a high-dose implantation of hydrogen ions in a material is heated. The gas pressure in the material causes microcavities, which are formed close to the implant range depth, to propagate and form fractures that cause the surface to blister and peel. By bonding the hydrogen-implanted wafer to a stiffening wafer prior to blistering, a transfer of a thin Si layer can be realized. To create the buried oxide layer, the wafer is simply oxidized prior to the hydrogen implantation, resulting in a transfer of both the buried oxide and Si after bonding. After bonding and cleaving of the SOI structure, a small amount of micoroughness remains, which is removed through chemomechanical polishing. This polishing does remove a fractional amount of the top layer thickness but can be compensated by altering the implant depth. A wide range of SOI layer thickness is possible due to the relative ease of hydrogen implantation in Si. The thickness is entirely dependent on the hydrogen implant energy (8 nm/keV), and, due to the very sharp implant profile, the dispersion is less than 8 nm over a 4-in wafer [18]. The implantation dose of hydrogen ranges from 2×10^{16} cm^{-2} – 1×10^{17} cm^{-2}. Unlike oxygen in the SIMOX process, hydrogen ions are relatively light and cause undetectable damage in the SOI layer. For this reason, defect densities in the SOI layer are equivalent to bulk material. An additional benefit of ion-cut is that the remaining Si, after blistering, can be reused for numerous ion-cut steps.

IV. Wafer Fabrication

The process presented for fabricating the reflecting substrates uses what can be referred to as a dual-modified ion-cut. The modification to the original ion-cut specification comes in the second stage process, where, instead of bonding an implanted substrate to a uniform Si substrate, it is bonded to another SOI substrate. A batch of 25 4-in wafers was fabricated using the dual-modified ion-cut technique. Fig. 2 shows the wafer fabrication steps.

Step 1) **Substrate A: Oxidation**

The first step in the process of creating the reflecting substrate using ion-cut technology is to oxidize a handle wafer. The oxide is thermally grown to a thickness of 437 nm as required by the $3/4\lambda$ DBR specifications. Due to properties of the thermal growth, uniformity can be achieved with a dispersion of less than 2.5%.

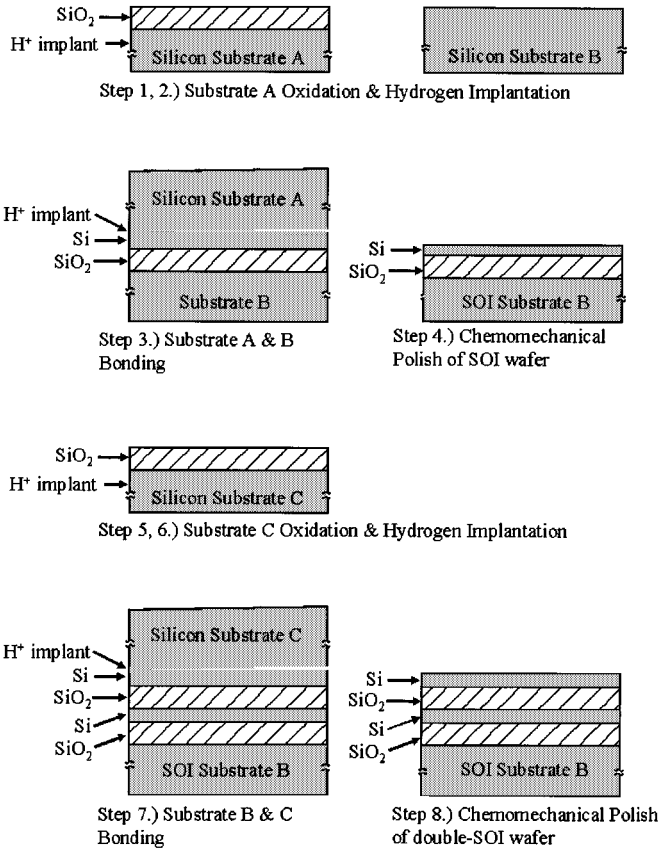

Fig. 2. Abbreviated double-SOI fabrication process showing second wafer bonding and substrate separation steps.

Step 2) **Substrate A: Hydrogen Implantation**

The next step is to implant the hydrogen ion-cut layer in the oxidized Si wafer. This implant will serve as the cleaving mechanism to achieve the SOI surface. This Si layer thickness is 174 nm, as calculated by the $3/4\lambda$ DBR requirements. The hydrogen is then implanted at a depth of approximately 610 nm below the SiO_2 surface or 174 nm below the Si–SiO_2 interface. The dispersion or straggle of the hydrogen implant is less than 8 nm since the stopping mechanism is primarily electronic.

Step 3) **Substrate A and B: Bonding**

Once the hydrogen implant is completed, a wafer bonding and ion-cut step is performed to achieve the thin SOI layer. Substrate A is pressed in contact to Substrate B at room temperature to form a hydrophilic bond. The contacted wafers undergo a two-step heat treatment to anneal the bond. In the first step, the wafers are heated to 400 °C–600 °C, which causes Substrate A to cleave at the hydrogen implant. This separates the bulk of Substrate A from the rest of the structure, the remaining material being reused for successive steps. The second step of the

heat treatment is performed at 1000 °C to strengthen the bond between the wafers.

Step 4) **Chemomechanical Polish**

The remaining structure is a completed SOI substrate. The completed structure is chemomechanically polished to remove the surface roughness that remains from the blistering process.

Step 5) **Substrate C: Oxidation**

Up until this point, the standard ion-cut process is followed. This process is repeated a second time with the modification of substituting the completed SOI wafer as the stiffening structure in the bonding step. Once again, an Si wafer is thermally oxidized to grow 437 nm of SiO_2 to serve as the second oxide layer in the DBR structure.

Step 6) **Substrate C: Hydrogen Implantation**

The hydrogen ion-cut layer is implanted to serve as the cleaving mechanism. The top Si layer thickness is 174 nm, so the depth of the implant will be approximately 610 nm below the SiO_2 surface or 174 nm below the Si–SiO_2 interface.

Step 7) **Substrate B and C: Bonding**

Next, Substrate C is bonded to Substrate B, which serves as the modified stiffening structure. The wafers are brought into contact at room temperature to form a hydrophilic bond. The contacted wafers once again undergo the two-step heat treatment. The first step heats the wafers to 400 °C–600 °C, causing Substrate C to cleave at the hydrogen implant. This separates the bulk of Substrate C from the rest of the structure with the remaining material being recycled. The second step of the heat treatment is performed at 1000 °C to strengthen the bond between the wafers.

Step 8) **Chemomechanical Polish**

The remaining structure is a completed reflecting substrate. The completed structure is chemomechanically polished to remove the surface roughness that is left after the blistering process.

V. Wafer Characterization

Crystalline quality characterization was performed using a Rigaku rotating anode X-ray machine and four-circle diffractometer to perform rocking curve analysis. In order to extract the crystalline quality of the surface layer and to decouple the underlying Si substrate, a grazing incidence X-ray scan was employed. Measurements of the surface Si device layer revealed a 0.166 48 ° rocking curve width. This compares with a 0.160 60 ° rocking curve width for a reference standard Si wafer. This measurement showed that within the experimental resolution, the two wafers were identical in crystalline quality and, therefore, suitable for Si epitaxy. A cross-sectional SEM of the double-SOI substrate is shown in Fig. 3. The substrate's reflectivity was specifically tuned to achieve a high reflectance at 850 nm for short haul optical communication systems. The reflectivity of this structure is seen in Fig. 4.

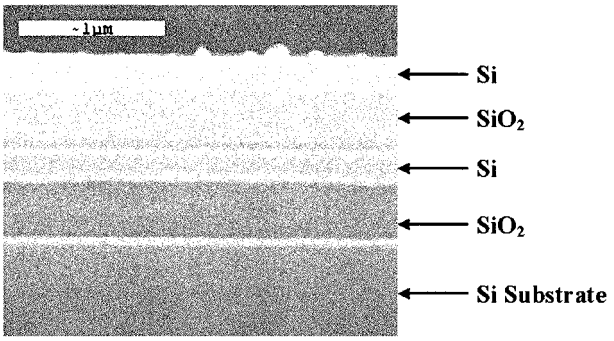

Fig. 3. Cross-sectional SEM of reflecting Si substrate showing buried distributed Bragg reflector.

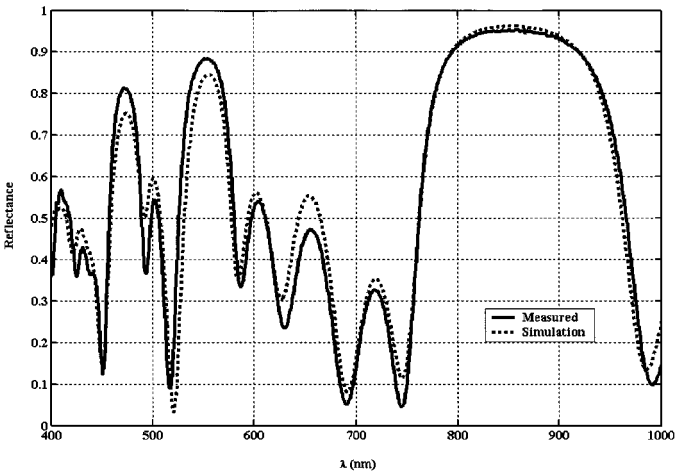

Fig. 4. Reflectivity of two period distributed Bragg reflector showing excellent fit with simulated results.

After the buried DBR fabrication, single crystalline Si was grown on the Si surface using a standard LPCVD epitaxy process. The surface Si layer was grown to approximately 2.1 μm in total thickness. The resulting structure has a reflectivity shown in Fig. 5. It can be seen in Fig. 5 that reflectivity is reduced to less then 40%, which could yield predicted photodiode quantum efficiencies in excess of 50%. It can also be seen in Fig. 5 that the minimum reflectivity, or maximum quantum efficiency, for photodiodes manufactured on these wafers would not be at the desired 850 nm wavelength.

Although the ion-cut manufacturing process can give strict thickness control, it is desirable that a technique be available for spectrally tuning the Si wafers. It has been shown that very-high-precision surface recessing can give desired spectral reflectance and, in turn, quantum efficiency [19]. We will simulate that through the use of surface recessing by means of Si etching, spectral tuning of the reflectance minimum can be achieved. Fig. 6 shows the simulated results of spectral tuning on the reflecting Si substrates through the recessing of the Si surface.

VI. Photodetector Fabrication

RCE p-i-n photodetectors were fabricated in the epitaxial device layer, which was approximately 2.1 μm in total thickness, using standard Si device fabrication techniques. The device structure is shown schematically in Fig. 7.

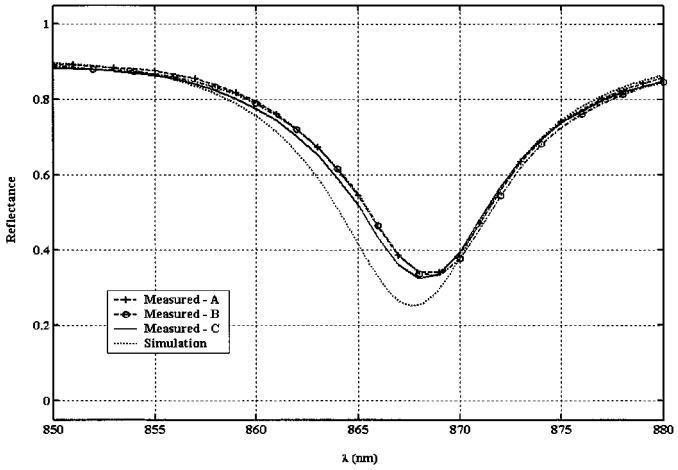

Fig. 5. Reflectivity of final Si wafer (acquired at three random locations on wafer) with buried DBR.

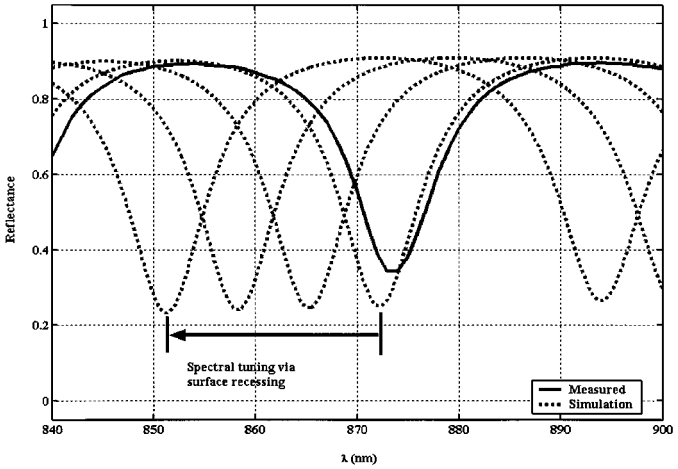

Fig. 6. Simulated effect of surface recessing for use in spectral tuning of the reflectance minima.

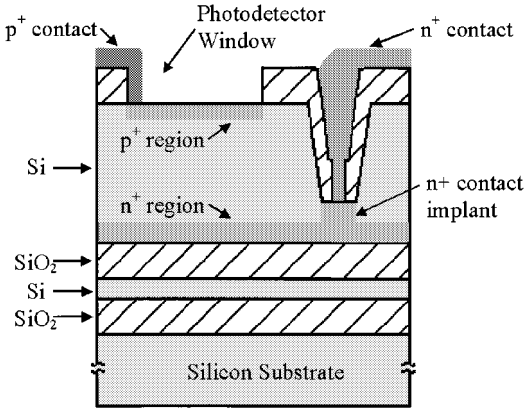

Fig. 7. Cross section of RCE Si p-i-n photodetector showing trench via for buried n^+ contact.

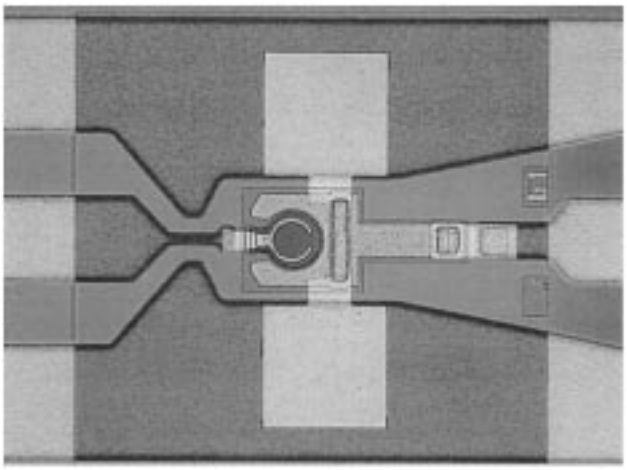

Fig. 8. Top view of finished photodetector showing coplanar transmission lines and coupling capacitors for dc biasing.

The structure has a buried n^+ implant and a p^+ implant on the surface, while the epitaxial Si layer is left undoped, yielding the vertical p-i-n diode. To contact the buried n^+ layer, a trench was formed using RIE technique with SF_6 reactant and He ambient. A high dose n^+ implant was then performed in the trench to achieve low contact resistance to the n^+ Si. Contacts were formed using Al patterned by a photoresist liftoff technique. For on-wafer high-speed testing, photodiodes with various dimensions were fabricated with coplanar transmission lines. A photo of the finished photodetector is seen in Fig. 8.

VII. Results and Discussion

The photodetectors were tested for dark current performance as well as for spectral quantum efficiency. The dark current as measured on 200-μm-diameter photodetectors varied from 1 to 3 μA/cm^2 at reverse bias of 1 to 3 V. On 30-μm-diameter devices, the dark current was measured as 10 and 17 μA/cm^2 at a reverse bias of 1 and 3 V, respectively. The increase in dark current density between the devices can be explained by surface effects, as the devices were not passivated in this study. An IV characteristic is seen in Fig. 9 for a 40-μm-diameter device with an ideality factor of approximately 1.6 under forward bias.

Spectral quantum efficiency measurements were performed using a tunable Ti:Sapphire laser source and a reference Si photodetector with known spectral responsivity for photocurrent normalization. It can be seen from Fig. 10 that the spectral quantum efficiency agrees well with the simulation and that the efficiency near 860 nm is approximately 40%, which corresponds to a responsivity of 0.260 A/W.

High-speed characterization is performed on a microwave probe station using a 50-GHz sampling oscilloscope to measure the photodetector response to 1.6-ps full-width at half-maximum (FWHM) pulses from a Ti:Sapphire laser source. Fig. 11 shows the temporal response obtained at 15 V reverse bias from 40-μm-diameter photodetector with measured FWHM value of 29 ps. The FWHM of 29 ps suggests a bandwidth above 10 GHz, which is well beyond the requirements for 10 Gbps data communications.

However, in these particular devices, a long tail in the photocurrent response is observed, indicative of a diffusion component. To limit the diffusion current due to absorption in doped neutral regions, we have used very thin (less than 0.2 μm) contact regions. The incomplete depletion of the unintentionally

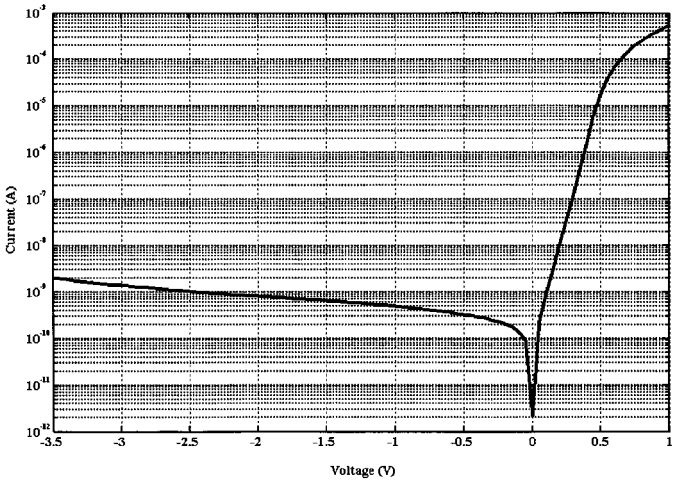

Fig. 9. IV characteristic for 40-μm-diameter device.

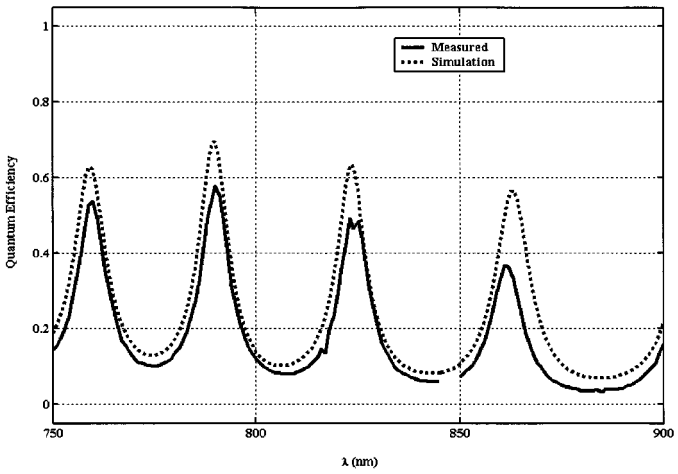

Fig. 10. Spectral quantum efficiency of RCE p-i-n photodetector.

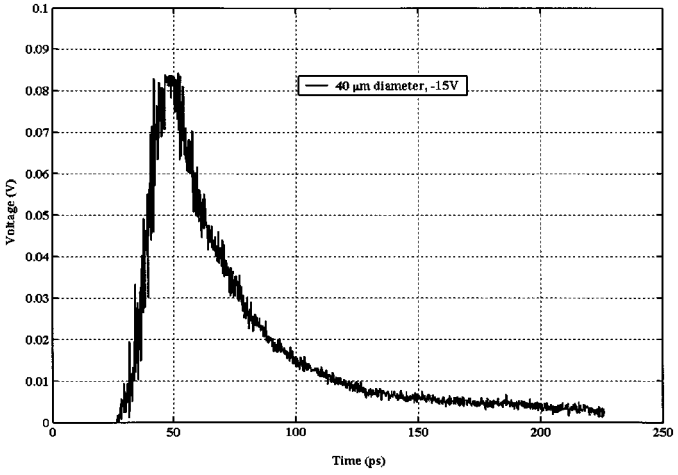

Fig. 11. Measured temporal responses of 40-μm-diameter photodiode.

doped absorption region is expected to be the main reason for the diffusion current and resulting reduction in the device speed.

To study the frequency response, measured temporal response data for various size devices at different bias values are converted to frequency domain using fast Fourier transform (FFT) as shown in Fig. 12. Fig. 13 shows the 3-dB bandwidth obtained from a 40-μm-diameter detector under different bias conditions.

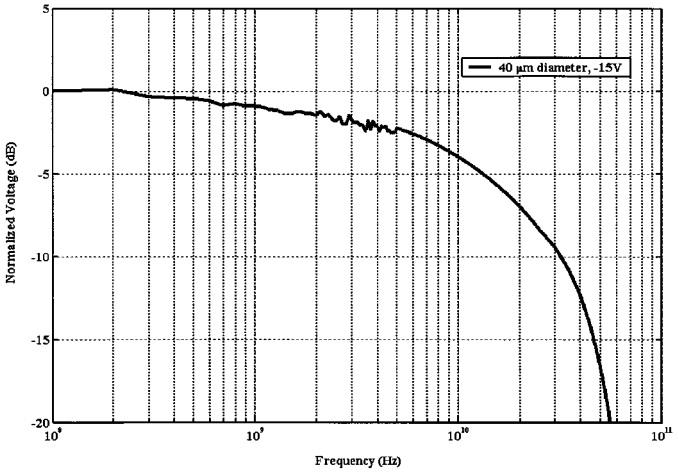

Fig. 12. FFT of temporal response for 40-μm-diameter photodiode at 15 V reverse bias.

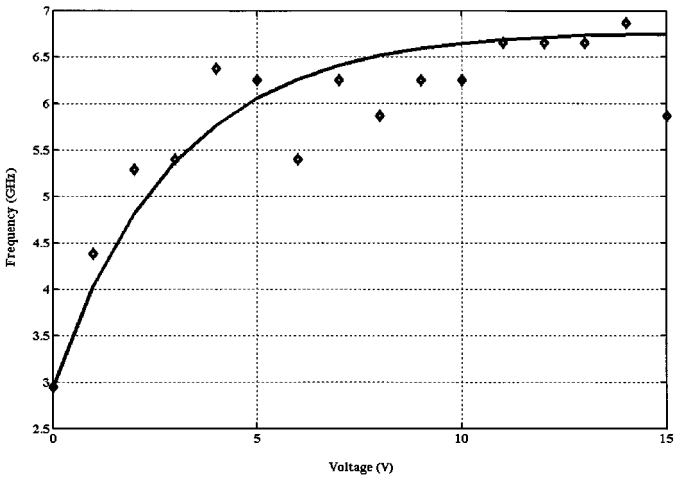

Fig. 13. 3-dB bandwidth as function of bias voltage for 40-μm-diameter photodiode (with trend line).

For all conventional photodetectors, the bandwidth-efficiency product is constant and depends on the absorption thickness, therefore, to increase the efficiency you must in turn sacrifice bandwidth. The benefit of an RCE structure is to increase the efficiency for a given absorption thickness detector while maintaining the bandwidth. The drawback of the RCE structure, however, is the wavelength selectivity of the photodetector efficiency. To counteract this selectivity and yet still benefit from the RCE structure, one can coat the top surface of the detector with an antireflection (AR) coating which will result in a "two-pass" detector where the light enters the photodetector and reflects off the buried mirror resulting in two passes of the absorption length. This will increase efficiency over a conventional detector while keeping the wavelength insensitivity over a substantial range. Fig. 14 shows the simulated responsivity-wavelength dependence of different absorption thicknesses as well as an 8-μm thickness with an

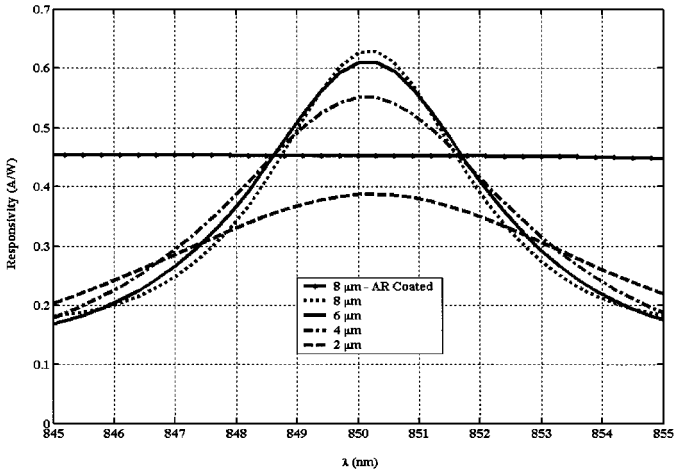

Fig. 14. Simulated responsivity for RCE photodetectors of different absorption lengths as well as 8-μm "two-pass" photodetector.

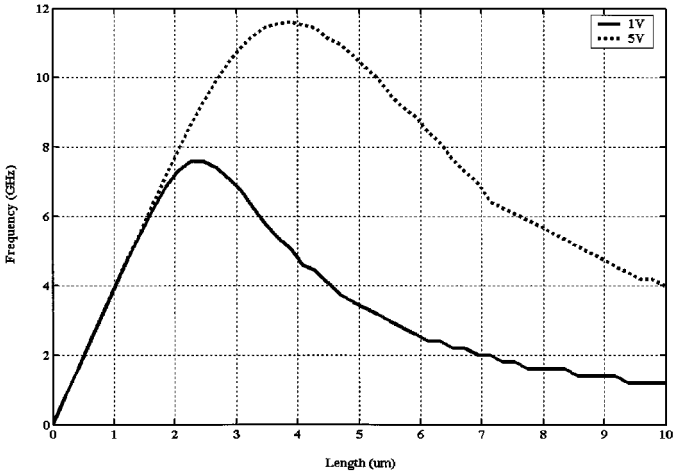

Fig. 15. Three-decibel bandwidth of a 100-μm-diameter photodetector with 1 and 5 V applied bias.

AR coating showing the wavelength insensitivity around 850 nm.

Just as increasing the absorption length will increase the efficiency, decreasing the absorption length will increase the bandwidth due to the reduction of carrier transit time. This effect is limited, however, as decreasing the absorption thickness will cause the photodetector capacitance between the N and P contacts to increase, resulting in the degradation of the device bandwidth. The goal of the designer is to find the optimal point for absorption length where capacitance and carrier transit time are minimized. The transit time of photodetectors is a function of the device length and the applied bias, as there is a relationship between carrier velocity and applied field. Fig. 15 shows the 3-dB bandwidth of a 100-μm-diameter detector with a 1- and 5-V applied bias. This simulation is performed by calculating the carrier velocity as a function of applied field as well as taking into account the device capacitance. From this information, time response is generated and then an FFT is carried out to calculate the frequency response, culminating in the calculation of the 3-dB bandwidth as a function of absorption thickness.

Future directions of this work will focus on Si–based detectors for long-haul communication wavelengths, specifically

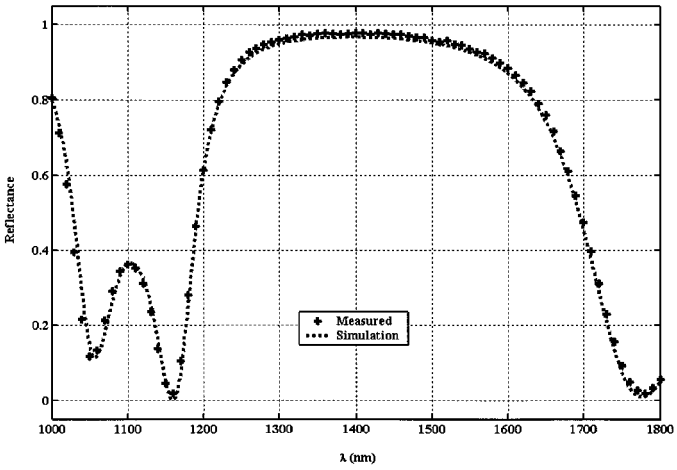

Fig. 16. Reflectivity of double SOI wafers for long-haul communication wavelengths.

1300 and 1550 nm. For these wavelengths, Ge on Si can be used as well as internal photoemission diodes such as SiGe or PtSi Schottky photodetectors [20]–[22]. We have also fabricated 6-in reflecting SOI wafers with buried DBRs for this application. Fig. 16 shows the reflectivity measurement for one of these wafers and its good agreement with the simulation. These wafers have in excess of 90% reflectivity over the wavelength range of 1300–1550 nm.

VIII. Conclusion

We presented commercially reproducible Si substrates with buried distributed Bragg reflectors having reflectivity over 90% for Si-based optoelectronics. We used the substrates to fabricate RCE Si pin photodetectors capable of quantum efficiencies above 40% at 860 nm and response times of 29 ps. The wafers could also be used to fabricate a host of Si-based integrated optoelectronics owing to the availability of Si processing and the availability of large wafer sizes. These wafers are well suited for VLSI integration and are compatible with standard CMOS processing, making them ideal for monolithic integration of receiver circuits with photodetectors. We have also introduced high-reflectivity Si substrates that cover the long-haul communication wavelengths (1300 and 1550) nm for use in Si-based photodetectors.

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