A 16 × 16 Multi-electrode Array with Integrated CMOS Amplifiers for Neural Signal Recording

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***Abstract*—This paper reports on an active 16 x 16, low-noise, low-power, multi-electrode array (MEA) neural sensor chip designed in IBM BiCMOS 8HP 0.13µm process with a total gain of 60 dB per input, a 20 kHz sample rate, an input-referred noise of 5.3 µVrms over 10 Hz to 10 kHz and a total power dissipation of 15.8 mW, or 61.7 µW per channel. A C4 microelectrode is attached to the input of each amplifier forming a multi-electrode array with 200 µm pitch for extracellular neural recording.**

I. INTRODUCTION

In vitro neural recording in tissue slices using multi-electrode arrays (MEA) is a powerful technique to study neuronal activity patterns that emerge in a network of cells [1,2]. High density, high count MEAs with sufficiently high sampling rates are in demand to be able to record activities in larger tissue slices. However, for a high density MEA, the electrode contacts may have to be placed only tens of microns away from each other. As the inter-electrode distance is approaching sizes comparable to that of a neuron and the number of electrodes is increasing to cover an area of the slice on the order of millimeter squares, running even a single metal line from each electrode to a distant amplifier becomes a challenging layout design problem.

Time multiplexing of multi-channel signals is a common technique that is often used to reduce the number of wires before transferring the signals to a site where they can be recorded and stored. However, neural signals need to be amplified up to millivolt levels before they can be safely sampled and multiplexed without compromising the signal quality. A potential solution to this design layout problem with high density MEAs is to build a micro amplifier next to each recoding contact and multiplex the signals out using fewer connections. This amplifier should satisfy certain design criteria as outlined below.

Extracellular neural signal amplitudes are typically from tens of microvolts to a few millivolts, with a bandwidth from sub-hertz for local field potentials to several kilohertz for single spike activity. The small amplitudes of these signals require an rms input-referred noise as small as 10 µV [3]. Additionally, the local temperature increase caused by the microsystem cannot exceed 1°C without causing damage to the surrounding neural cells; this requirement demands minimal power dissipation from the microsystem. A compact integration area is necessary to increase the number of recording electrodes per unit area for high spatial resolution of neuronal measurements; this leads to more noise and increased power consumption. The challenge of designing such a neurosensor lies in maximizing the amplification of low-level signals and using the minimum area necessary while keeping electronic noise sufficiently below the level of the extracellular signals.

This paper reports on the design and simulation of a multiple-input neural sensor integrated circuit (MINS IC) chip that explores the use of C4 bumps as a novel MEA. A C4 bump is a semi spherical solder ball, usually used in flip-chip bonding, for interconnecting semiconductor devices to external circuitry. The merit of using C4 bumps as probes is that they are compatible with the standard CMOS process, thus requiring minimal post-processing of the active MEA chip.

II. ACTIVE MULTI-ELECTRODE ARRAY NEURAL SENSOR CHIP ARCHITECTURE

The architecture of the active MEA neural sensor chip is illustrated in Fig. 1. It consists of an MEA of 16 x 16 (256) C4 bumps for extracellular recordings of neural activity. Each C4 bump is connected to an individual low-noise pre-amplifier. The row scanning circuit (RSC) repeatedly generates non-overlapping pulses to cycle through all 16 pre-amplifier rows in each of the 16 columns, one row at a time from row 0 to row 15. Each row is selected for 3.125 µs to obtain a sample rate of 20 ksps for each electrode in the whole array.

A current conveyor is used as the second stage for each of the 16 columns to achieve an overall gain of 60 dB and simultaneously keep the voltage of each column at a constant level. Two 8-to-1 analog multiplexers convert 16 columns into 2 analog outputs in order to minimize the I/O count. Synchronized clocks are generated by on-chip frequency dividers from a single off-chip clock to control both the RSC and the analog multiplexers, thus realizing 256 parallel inputs with just two time-division multiplexed outputs. The architecture was designed to be able to increase the number of amplifiers with a minimum increase in output connections and power requirements.

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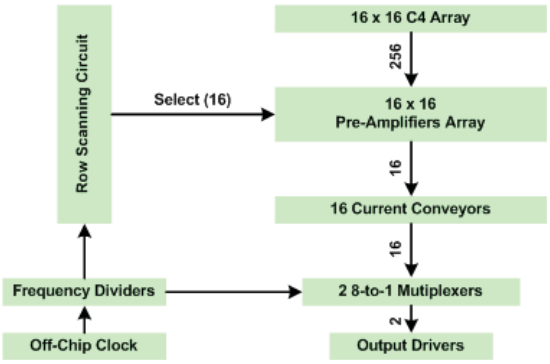

Fig. 1 Active multi-electrode array neural sensor chip architecture

III. ACTIVE MULTI-ELECTRODE ARRAY NEURAL SENSOR CIRCUIT DESIGN

A. Pre-Amplifier

The schematic of the pre-amplifier is shown in Fig. 2. The pre-amplifier is a PMOS cascode amplifier, consisting of M_1 and M_2, with a 10 pF input coupling capacitor. The transistor M_2 is also used as a switch to enable the entire row when selected. M_0 is used as a high-impedance pseudo-resistor to bias the gate of M_1 at the voltage V_1, allowing the low frequency pole to be tuned down to the sub-hertz range [4, 5]. An adjustable off-chip current source will be used to compensate for process variation from chip to chip. All 16 pre-amplifiers in a column share the same NMOS transistor M_3 as a current source. The dashed box in Fig. 2 is an additional pre-amplifier which will be used during calibration mode. Switch S1 is used as part of the calibration procedure. The output of the all the pre-amplifiers in a column is fed into a single current-conveyer.

B. Current Conveyor

Fig. 3 illustrates the schematic of the current conveyor. This current conveyor is a current amplifier followed by a transimpedance structure (M_{16}-M_{19}) and an NMOS source follower. With a differential input stage and negative feedback to the non-inverting input, the DC bias voltage of the non-inverting input is forced to follow the voltage of V_2, which is generated from an on-chip voltage reference [6]. Keeping the negative input of the current conveyor at a constant voltage is critical because the inverting input is also the voltage of the column lines of the pre-amplifier array. This is because the signals generated by the shift register to turn M_2 on and off for each row are non-overlapping. Thus, there will be a short time that all the cell amplifiers in a column are shut down. The existence of this column amplifier will prevent the voltage of the column line from dropping to ground, which would slow down the scanning speed of the circuit and cause spikes on the signal waveforms.

The signal current is replicated by M_{12} and M_{14}, and converted back into the voltage domain by M_{17} and M_{19}. Also, a compensation feedback resistor R_c = 2.86 kΩ and capacitor Cc = 1 pF are used to improve the stability of the current conveyor.

C. Row Scanning Circuit

The schematic of the RSC is shown in Fig. 4. Compared to the analog multiplexer, which handles the columns, the RSC provides controls for picking one of the sixteen rows during the readout mode. As shown in Fig. 4, the main blocks of the RSC are data flip-flops (DFF), which are used to construct both dividers and a shift register.

Reset' is utilized to write the initial state into the shift register and dividers, which are also used to control the analog multiplexer. When Reset' is enabled, the pre-amplifier in row 0 and column 0 will be selected. There are two operation modes for the pre-amplifier array: calibration mode and readout mode, which is mediated by the RSC. In the calibration mode, Cal' (complementary Cal signal) goes low, V_{Row0} to V_{Row15} go high, and all the rows are shut off; V_{cal} goes low and the calibration pre-amplifiers are turned on; V_{re} (gate voltage of M_0, Fig. 2) goes low, the PMOS pseudo-resistors are forced to a low-impedance state, which results in the gate voltage of M_1 to be recalibrated to V_1.

When Cal' goes high, readout mode is resumed. In readout mode, two modalities exist: continuous and stop mode. The difference between these two modes is that during the continuous readout mode all the rows are selected one after another from row 0 to row 15 repeatedly, while during the stop mode only one row is enabled throughout the whole stop mode period. Stop mode is enabled when Stop' is low. Waveforms of different operation modes are illustrated in Fig. 5.

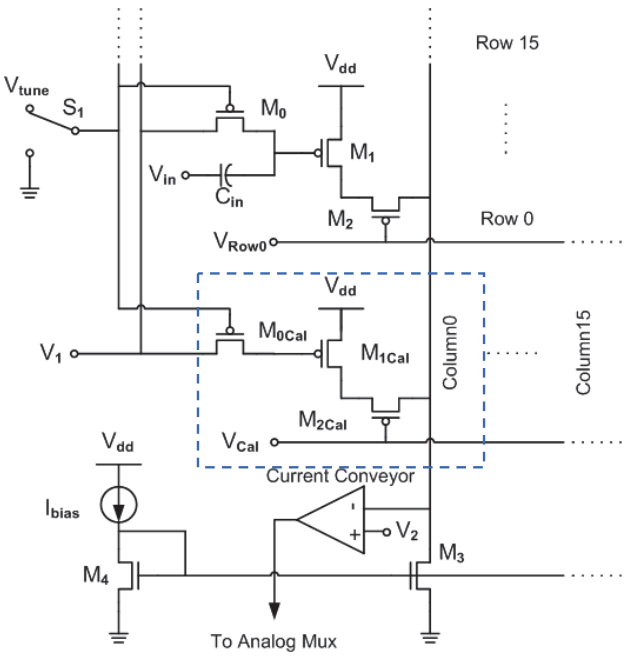

Fig. 2 Schematic of the pre-amplifier

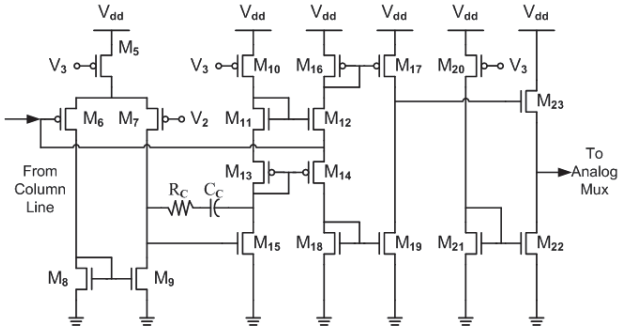

Fig. 3 Schematic of the current conveyor

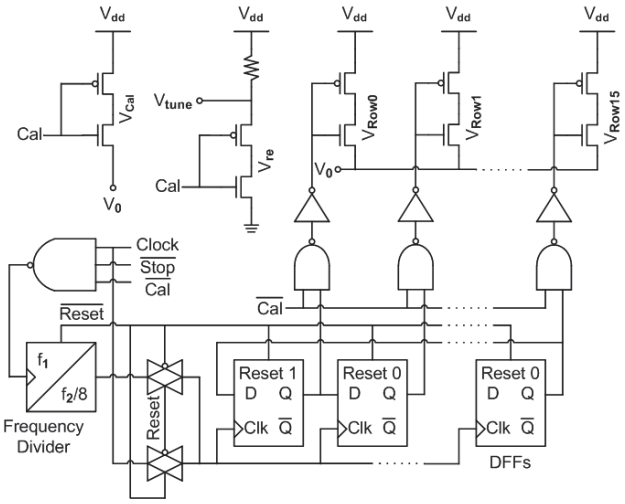

Fig. 4 Schematic of the row scanning circuit

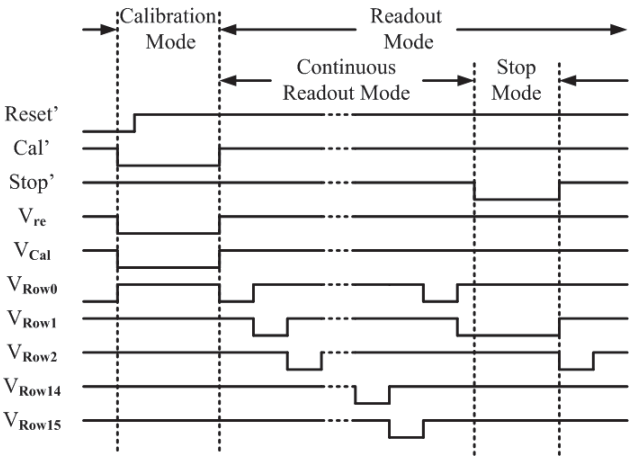

Fig. 5 Row scanning circuit control signal waveforms during different operation modes

IV. SIMULATION RESULTS

The active MEA neural sensor chip was designed and fabricated using IBM BiCMOS 8HP 0.13µm technology with 5 levels of metal interconnections. The complete layout, measuring 4 mm by 4 mm, is shown in Fig. 6. Both schematic based and layout based simulations were done using Spectre from Cadence IC 6.14. A voltage gain of 52.9 dB was achieved by using only the pre-amplifier without the successive current conveyor. Input and output voltage waveforms are depicted in Fig. 7.

The current conveyor plays the most important role in improving the stability of the whole system since it is the only circuit block that uses negative feedback. The stability of the current conveyor has been studied by simulating its phase margin. The circuit's voltage gain and phase are plotted in Fig. 8 as a function of frequency. A phase margin of 86° was achieved by employing the RC compensation technique as shown in Fig. 3.

The entire active MEA neural sensor chip was simulated using schematic models, with a 15 pF capacitor as the output load. An input stimulus of 1 kHz, 20 µV peak-to-peak sinusoidal signals were applied as an input to pre-amplifiers (0, 0), (0, 1) and (0, 2), in which the x-coordinate is the pre-amplifier's row number and y-coordinate is its column number. Inputs to all other pre-amplifiers were connected to ground. The output data was collected and the time-division multiplexed signal from input (0,2) was reconstructed and plotted in Matlab. The reconstructed waveform from input (0, 2) is shown in Fig. 9. Table I listed the comparison of this work and similar neurorecording chips reported in literature. The neural sensor chip presented in this paper has a high count MEA, in which all channels can be continuously monitored, while retaining low noise and low power. Lower noise was presented in [1], but with a power budget almost an order magnitude greater than this work.

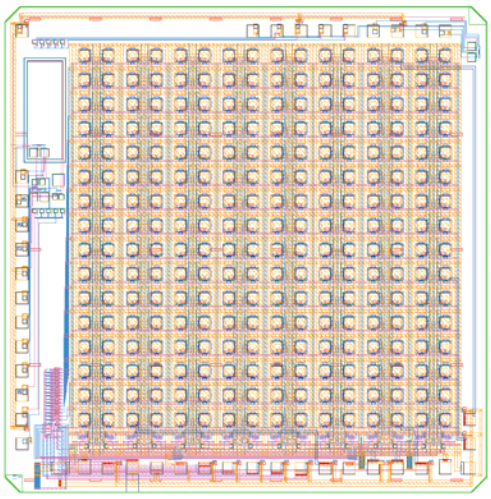

Fig. 6 Active multi-electrode array neural sensor chip layout

TABLE I. COMPARISON OF THIS WORK WITH PREVIOUS DESIGNS

	Frey [1]	Imfeld [2]	Aziz [3]	Sodagar [5]	Evermann [6]	Present Work Simulation Results
No. of channels	126	4096	256	64	16384	256
Voltage gain	0 dB ~ 80 dB	55 dB[b]	60 dB	60 dB	N/A	60 dB
Input referred noise	2.4 μVrms[a] (1 Hz - 100 kHz)	11 μVrms (10 Hz - 100 kHz)	7 μVrms (1 Hz - 5 kHz)	8 μVrms (100 Hz - 10 kHz)	N/A	5.3 μVrms (10 Hz - 10 kHz)
Power consumption	135 mW @ 3.3 V/ 5 V 1.07 mW/Ch.	132 mW @ 3.3 V 32.2 μW/Ch.	5.04 mW @ 3 V 15 μW/Ch.	14.4 mW @ 1.8 V 225 μW/Ch.	656 mW @ 5 V 40 μW/Ch.	15.8 mW @ 2.5 V 61.7 μW/Ch.
Process	0.6 μm CMOS	0.35 μm CMOS	0.35 μm CMOS	0.5/1.5 μm CMOS	0.5 μm CMOS	0.13 μm BiCMOS

a. Front-end input referred noise
b. Minimum amplification.

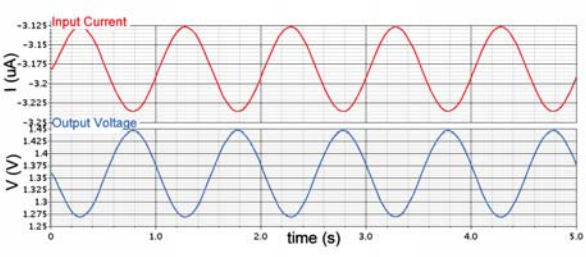

Fig. 7 Transient simulation results of a single pre-amplifier

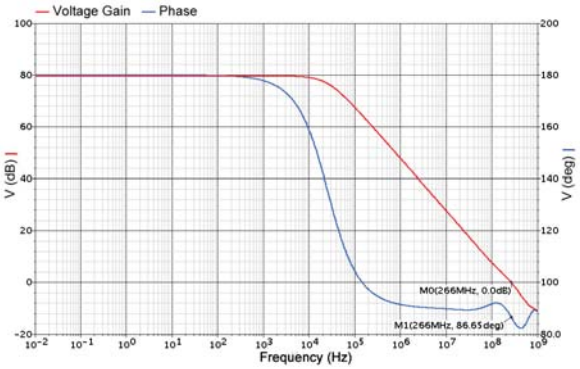

Fig. 8 Frequency response of the current conveyor

V. CONCLUSION

The design and simulation results for an active, low-noise, low-power, 60-dB, 256-input MEA chip for neural recording based on a 2.5-V 0.13 μm BiCMOS process has been presented. No bipolar devices were used in the design, thus this chip is completely CMOS compatible. A 4 x 4 mm^2 chip was fabricated by MOSIS as part of the MOSIS Educational Program (MEP).

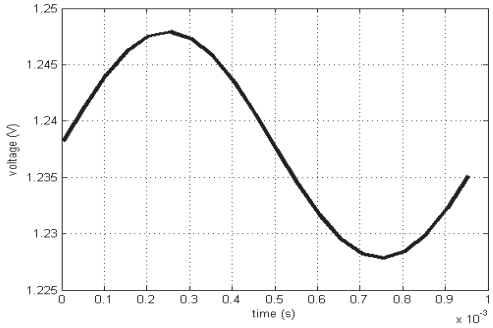

Fig. 9 Reconstructed output waveform of a 1 kHz sinusoidal signal

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