

GaAs-Si heterojunction bipolar transistor

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(Received 24 November 1987; accepted for publication 4 January 1988)

A GaAs/Si heterojunction bipolar transistor (HBT) structure is proposed having application for high-frequency operation. The structure combines the high-frequency capability of the GaAs/AlGaAs system with the advanced processing technology of Si. The proposed device consists of an n -AlGaAs/ p -GaAs emitter and base layers on an n -Si collector with improved junction characteristics at the GaAs/Si heterointerface afforded by thermal annealing. This novel device structure combines the advantages associated with a wide band-gap AlGaAs emitter, the high electron mobility of GaAs, and the substantial reduction in device parasitics accorded the self-aligned structure. Additionally, the proposed device offers the possibility of planar GaAs processing. With the use of a compact transistor model, calculations of the high-speed capability of this transistor are presented. For an emitter-base junction area of $1\ \mu\text{m} \times 5\ \mu\text{m}$, optimized $f_{\text{max}} = 108\ \text{GHz}$ and $f_{\text{max}} = f_t = 89\ \text{GHz}$ were computed for the GaAs/Si HBT, compared to 76 and 62 GHz, respectively, for equivalent GaAs/AlGaAs HBT's.

Bipolar transistors have attracted much attention recently as promising devices for high-speed microwave and digital applications. Through the development of various super self-aligned techniques, impressive reductions in device parasitics have been achieved in the speed of Si homojunction bipolar transistors.^{1,2} However, with Si bipolar transistors approaching the high-frequency potential of the semiconductor material property, substantial further advances in speed from additional reductions in device dimensions are not anticipated. Considerable efforts are therefore being directed towards the GaAs/AlGaAs heterojunction bipolar transistor (HBT)³⁻⁶ as superior high-frequency performance is expected from the higher electron mobility of GaAs and the higher base doping level permitted by the wide band-gap AlGaAs emitter.^{7,8} Practically limited by device parasitics, the development of several self-alignment techniques has recently realized devices exhibiting extrapolated $f_t = 55\ \text{GHz}$ and $f_{\text{max}} = 105\ \text{GHz}$.⁶

The rapidly advancing GaAs-on-Si technology has reported many achievements in recent years,⁹ among which include the successful realization of a GaAs/AlGaAs HBT on Si.¹⁰ Yet pursuing improved quality in the epitaxially grown GaAs, investigators have recently demonstrated the notable success of thermal annealing in reducing dislocation densities near the GaAs-Si heterointerface.¹¹ Studying the electrical properties of annealed p -GaAs/ n -Si heterojunction diodes, Ünlü *et al.*¹² have reported ideality factors of 1.5 and reverse leakage currents of $10^{-3}\ \text{A/cm}^2$ at 5 V. Encouraged by the quality of the annealed heterointerface, approaching that of a GaAs p/n homojunction, in this letter we propose an integrated GaAs and Si HBT. Combining the intrinsic high-performance potential of the GaAs/AlGaAs HBT with the advanced planar processing technology of Si, a novel self-aligned device structure is designed which exhibits potentially superior performance. The unique processing steps needed to realize the proposed device structure will be discussed, and calculations of its high-speed capability will be presented.

A schematic representation of the proposed device structure is shown in Fig. 1. The particular GaAs/Si HBT structure studied consists of a wide-gap n -AlGaAs emitter layer and a high-mobility p^+ -GaAs base layer on an epitaxial n -Si collector layer. By employing conventional Si processing techniques, a n^+ buried layer is diffused into a p -Si substrate followed by the epitaxial growth of the n -Si collector. Fully recessed oxide isolation regions are then formed by selective thermal oxidation. A thin, $0.1\ \mu\text{m}$ chemical vapor deposited (CVD) SiO_2 film is deposited and etched to reveal the collector contact windows. $0.15\ \mu\text{m}$ of undoped polycrystalline silicon (polysilicon) is subsequently deposited on the entire surface and selectively oxidized. Base electrode regions are defined by implantation of boron ions into the polysilicon, while arsenic ions are implanted for the collector electrodes. Finally, a thin Si_3N_4 etch stop film is deposited, and active device areas are etched down to the Si collector.

After the Si processing, the GaAs/AlGaAs epitaxial layers are selectively grown in a self-aligned fashion by molecular beam epitaxy.^{13,14} With a choice of parameters characteristic of typical GaAs/AlGaAs HBT's, the p^+ -GaAs base layer is designed to be $0.1\ \mu\text{m}$ thick, the $n\text{-Al}_{1-x}\text{Ga}_x\text{As}$ emitter layer $0.2\ \mu\text{m}$ thick with an Al mole fraction $x = 0.3$, and the n^+ -GaAs cap layer $0.1\ \mu\text{m}$ thick.⁵ Subsequent to growth, *ex situ* thermal annealing of the p -GaAs/ n -Si heterointerface is performed as described by Ünlü *et al.*¹² Alternatively, additional studies are under way to determine the feasibility of *in situ* annealing of the GaAs/Si heterointerface¹⁵ prior to growth of the n -AlGaAs emitter layer.

The patterned emitter contact metal is deposited and used to mask the wet chemical etching of the polycrystalline GaAs/AlGaAs layers grown on the Si_3N_4 film. Meanwhile, contact to the base is achieved laterally via the "buried" pre-deposited polysilicon. Finally, device fabrication is completed by conventional processing steps. Namely, a $0.5\text{-}\mu\text{m}$ -thick CVD SiO_2 film is grown, vias are opened through the SiO_2 and Si_3N_4 etch stop film, and overlay metal is deposited

producing emitter, base, and collector bonding pads.

The device structure shown in Fig. 1 offers several advantages with respect to high-speed performance, planar device processing of GaAs, and integration of GaAs and Si. Similar to the GaAs/AlGaAs HBT, the wide band-gap emitter of the present structure offers several advantages over the Si homojunction bipolar transistor, as discussed by several authors.^{7,16} Additionally, the high electron mobility of GaAs contributes to a lower minority-carrier base transit time.

In addition to the typically cited advantages of GaAs-on-Si technology,⁹ the GaAs/Si HBT can uniquely avail the advanced planar processing techniques of Si. In contrast to the stepped collector, base, and emitter mesa structures characteristic of III-V compound semiconductor technology, the Si processing technique employed in the present structure produces a relatively flat surface topography. The highly planar surface eases the formation of the active region opening and the subsequent emitter mesa definition. Additionally, large-scale integration is facilitated, while monolithic integration with Si-based devices is also enhanced by the reduced step height.

With the use of only a single noncritically aligned mask, the base and emitter regions are defined in a super self-aligned fashion as the base and emitter layers are consecutively grown in the same etched window. Herein lies both the primary advantage of the GaAs/Si HBT as well as the potential limitation of this device. Through the resultant elimination of the extrinsic GaAs base region, superior speed-power performance is expected from the minimization of the extrinsic base resistance and collector-base capacitance contributions, although the polysilicon sheet resistance and collector-base SiO₂ capacitance must be appropriately accounted for. Meanwhile, the feasibility of selectively growing GaAs on Si with $\sim 1 \mu\text{m}$ dimensions will require further investigation. This technique, however, has been demonstrated over larger dimensions.¹³

To evaluate the high-speed performance of the proposed *n*-AlGaAs/*p*-GaAs/*n*-Si HBT, the current gain cutoff frequency f_i and the maximum oscillation frequency f_{max} were calculated by using a compact transistor model commonly

used for Si microwave transistors.¹⁷ The emitter-to-collector transit time τ_{ec} is modeled as the sum of the emitter depletion-layer charging time τ_e , the base-layer transit time τ_b , the collector depletion-layer transit time τ_{SCL} , and the collector depletion-layer charging time τ_c . The effective base resistance-collector capacitance time constant τ_{eff} is given by the base contact resistance R_{bc} , the intrinsic and extrinsic base resistances, R_{bi} and R_{bs} , respectively, and the intrinsic and extrinsic collector capacitances, C_{ci} and C_{cs} , respectively.⁸

Before analyzing the proposed GaAs/Si structure, the predictions of our device model were verified with the best reported theoretical and experimental results. For the "ideal" GaAs/AlGaAs structure studied by Sunderland and Dapkus,⁸ close agreement between the models was observed in the computed figures of merit. Similarly, analysis of the GaAs/AlGaAs HBT experimentally studied by Chang *et al.*⁶ also showed excellent agreement. With a notable 600-Å-thin, $1 \times 10^{20} \text{ cm}^{-3}$ doped base layer, extrapolated f_i of 55 GHz and f_{max} of 105 GHz were obtained. These values compare well with the predicted values of 47 and 107 GHz, respectively.

Calculations were performed on the designed structure for a device with a $1 \times 5 \mu\text{m}^2$ emitter area, operating at a collector current density of $5 \times 10^4 \text{ A/cm}^2$ and a collector-base reverse bias of 5 V. By using a presumed specific contact resistance value of $1.0 \times 10^{-7} \Omega \cdot \text{cm}^2$ for the *p*-GaAs, doping concentrations were varied to optimize the figures of merit. In Table I are listed the design parameters and calculated performance of the proposed Al_{0.3}Ga_{0.7}As/GaAs/Si device. For comparison, an equivalent Al_{0.3}Ga_{0.7}As/GaAs/Al_{0.3}Ga_{0.7}As HBT was also modeled by using a conventional self-aligned base with a 0.25 μm extrinsic base spacing. For a 1000-Å-thick base doped $1.0 \times 10^{19} \text{ cm}^{-3}$, f_{max} was optimized at a value of 108 GHz for the GaAs/Si HBT, as compared to 76 GHz for the GaAs/AlGaAs HBT. (While significantly higher values of f_{max} may be simulated for both structures by increasing the base doping, a maximum doping concentration of $1.0 \times 10^{19} \text{ cm}^{-3}$ was imposed

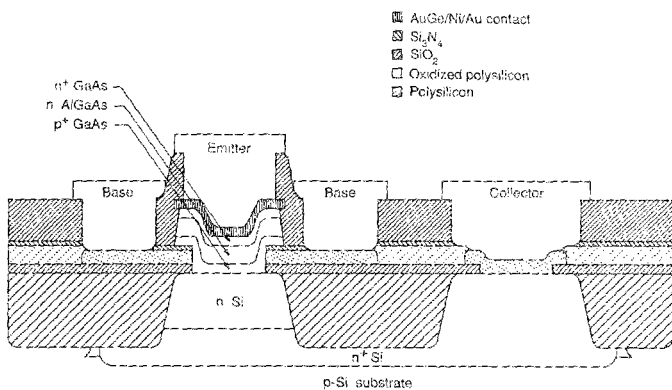


FIG. 1. Schematic drawing of the proposed *n*-AlGaAs/*p*-GaAs/*n*-Si heterojunction bipolar transistor structure.

TABLE I. Device performance and parameters.

	AlGaAs/GaAs/Si		AlGaAs/GaAs/AlGaAs	
N_E (cm^{-3})	2×10^{17}	2×10^{17}	2×10^{17}	2×10^{17}
N_B (cm^{-3})	1×10^{19}	1×10^{19}	1×10^{19}	1×10^{19}
N_C (cm^{-3})	7×10^{16}	1×10^{18}	7×10^{16}	3×10^{17}
C_e (fF)	11.0	11.0	10.7	10.7
C_{ci} (fF)	1.5	6.2	1.4	2.9
C_{cs} (fF)	2.1	2.1	7.9	15.9
R_{bi} (Ω)	11.0	11.0	11.0	11.0
R_{bs} (Ω)	29.7	29.7	27.5	27.5
R_{bc} (Ω)	19.4	19.4	16.3	16.3
τ_e (ps)	0.15	0.18	0.21	0.31
τ_b (ps)	1.34	1.14	1.34	1.27
τ_{SCL} (ps)	1.88	0.44	1.95	0.97
τ_c (ps)	0.05	0.03	0.02	0.01
τ_{ec} (ps)	3.42	1.80	3.51	2.56
τ_{eff} (ps)	0.16	0.44	0.32	0.64
f_i (GHz)	46	89	45	62
f_{max} (GHz)	108	89	76	62

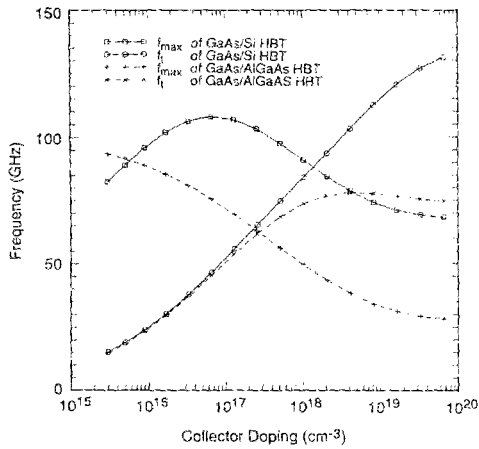


FIG. 2. f_i and f_{max} as a function of the collector doping concentration for the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}/\text{Si}$ and $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}/\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ transistors. The emitter and base doping concentrations are 2×10^{17} and $1 \times 10^{19} \text{ cm}^{-3}$, respectively. Calculations were done for $J_c = 5 \times 10^4 \text{ A/cm}^2$ and $V_{cb} = 5 \text{ V}$.

as a practical limit for consistently realizable structures.) As a possibly more meaningful figure of merit, the optimized performance at which f_{max} equals f_i is also reported, since useful transistors are limited by the power gain limitations specified by f_{max} and the impedance matching restrictions characterized by f_i . By independently optimizing the GaAs/Si and GaAs/AlGaAs HBT structures, computed values of 89 and 62 GHz were obtained, respectively, as detailed in Table I and clearly illustrated in the frequency versus collector doping plot presented in Fig. 2.

Substantial reductions in R_{bs} and C_{cs} are expected from the use of polysilicon sidewall contacts in this novel self-aligned device structure. Ideal device performance, however, is yet limited by the resistance of the polysilicon base contact and the collector capacitance of the thin SiO_2 layer. As evidenced in the R_{bs} values presented in Table I, the $70 \Omega/\square$ sheet resistance of the thin $0.15 \mu\text{m}$ base polysilicon sufficiently degrades performance such that no significant improvement in R_{bs} is observed in spite of the self-aligned contact. Additionally, the thin $0.15\text{-}\mu\text{m}$ -wide polysilicon contact to the base in fact gives rise to a contact resistance R_{bc} value greater than that of GaAs/AlGaAs structures, where $1\text{-}\mu\text{m}$ -wide contacts are typically used. With silicide sheet resistances $\sim 1 \Omega/\square$, however, dramatic reductions in extrinsic base resistance is expected with modeled f_{max} values approaching 143 GHz.

Having removed the conventional collector-extrinsic base capacitance, the extrinsic collector capacitance C_{cs} is governed only by the thin, $0.1 \mu\text{m}$ SiO_2 film separating the base polysilicon from the $n\text{-Si}$ collector. This capacitance contribution is observed to produce a dramatically reduced C_{cs} , which is a dominant factor in the τ_{eff} term, and therefore greatly improves f_{max} . In addition, the reduction in C_{cs} further improves f_{max} by significantly decreasing the charging time τ_c , and thereby increasing f_i and f_{max} (f_i).

Finally, minor differences in time constants and intrinsic capacitances are realized as a consequence of the material

properties of the Si collector. With a lower dielectric constant, a lower built-in voltage, and a higher saturation velocity than $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$, the Si collector produces a slight reduction in τ_{SCL} and a slight increase in C_{ci} . These intrinsic components, however, are more strongly dependent upon doping concentration, as illustrated in Fig. 2.

In conclusion, a novel GaAs/Si heterojunction bipolar transistor structure has been proposed integrating the superior characteristics of a GaAs/AlGaAs HBT with the advanced planar processing technology of Si. With the use of Si super self-aligned techniques, details on a possible processing of the device have been outlined, including the selective self-aligned growth of the GaAs/AlGaAs epitaxial layers. Modeling the microwave performance of this device, a maximum $f_{max} = 108 \text{ GHz}$ was predicted, while an optimized value of 89 GHz was simulated at which $f_{max} = f_i$. These high-speed performance values are very encouraging, as they are superior to values predicted for realizable GaAs/AlGaAs HBT's with equivalent design parameters. Finally, as optimum design parameters were not used in the present simulations, potential improvements should be realized in this structure as GaAs and Si processing techniques are further developed.

The authors would like to thank J. Brighton of Texas Instruments and G. Munns for helpful discussions. This work is supported by grants from the U.S. Air Force Office of Scientific Research, Sperry, Texas Instruments, and Ford Aerospace.

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