

# Realization of High-Efficiency 10 GHz Bandwidth Silicon Photodetector Arrays for Fully Integrated Optical Data Communication Interfaces

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## Abstract

We present a commercially reproducible fabrication technique for producing high quantum efficiency photodiodes with up to 10 GHz bandwidth on double silicon-on-insulator (SOI) wafers. The substrate consists of a two-period distributed Bragg reflector (DBR), which provides a 90% reflecting surface. Resonant-cavity-enhanced (RCE) Si photodetectors with 40% quantum efficiency at 860 nm and a FWHM of 29 ps suitable for 10 Gbps data communications are demonstrated. We also demonstrate integrated photodiode arrays in silicon substrate for multi-channel high speed serial interfaces.

## 1. Introduction

The needs for high-speed optical backplane solutions and high-bandwidth chip-to-chip data communication interfaces are becoming increasingly prominent with the rapid evolution of processor clock frequencies and the raw processing speed. In fact, typical processor speed has been increasing much faster than typical on-board bus data rate over the last two decades, and the gap between processor clock frequency and bus data rate in conventional systems is about one order of magnitude today. This gap represents a significant bottleneck in the design of high performance systems. It is expected that high-speed serial data communication interfaces and opto-electronic data bus architectures will be explored vigorously to answer these needs in the near future.

The efforts to create fully integrated high-speed photodiodes and opto-electronic interfaces for serial data communication on-chip have been impeded, however, by the fact that silicon photodiodes typically have a very low quantum efficiency at wavelengths (800-900 nm) used for short distance fiber optic links. In this paper, we present a viable fabrication technique for producing high quantum efficiency photodiodes with up to 10GHz bandwidth on SOI wafers, discuss high-speed measurement results, and demonstrate integrated photodiode arrays in silicon substrate for multi-channel high speed serial interfaces. The technology and the components presented here are compatible with standard CMOS process, making them well suited for monolithic integration of receiver circuits. Figure 1 shows the conceptual block diagram of a monolithic multi-channel system interface where an array of integrated photodetectors are

used to receive the optical input signals, and the transimpedance / limiting amplifiers as well as the clock-data recovery (CDR) circuitry complete the high-speed link to the digital core circuits.

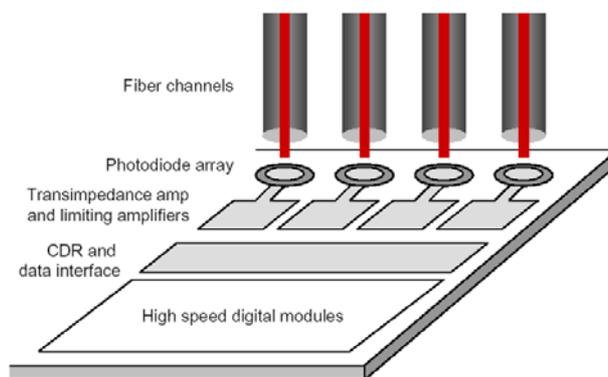


Fig. 1: Conceptual block diagram of an integrated multi-channel photo-receiver array for data communication.

Resonant-cavity-enhanced (RCE) photodetectors have been the focus of extensive research over the past decade in the design of high bandwidth-efficiency product devices [1,2]. Silicon-based photodetectors for applications in optical communications in the near-IR wavelength range between 800-900 nm suffer from low bandwidth-efficiency products due to the long absorption length necessitated by the small absorption coefficient. Increasing the bandwidth-efficiency product is the inherent benefit of a RCE structure, which relies on the constructive interference of a Fabry-Perot cavity to enhance the optical field inside the photodetector at specific wavelengths. For semiconductor photodetectors, such a resonant cavity can be formed using a buried reflector consisting of alternating layers of semiconductors and the air/semiconductor top interface. Due to the availability of heterostructures, compound semiconductors have been the focus of RCE photodetector development [1]. Formation of buried mirrors and resonant cavities have remained as a challenge in Si technology.

Various attempts to fabricate Si RCE photodetectors included chemical vapor deposition (CVD) as well as molecular beam epitaxy (MBE) [3] of Si on top of di-

electric mirrors, which resulted in a polycrystalline device layer, due to the amorphous seed layer. Photodiodes fabricated on a polycrystalline device layer typically suffered from high dark currents. Schaub et al. [4], has reported silicon RCE photodiodes with low dark currents that achieved a bandwidth in excess of 34 GHz – the highest speed recorded for Si pin photodiodes. Although the merged epitaxial layer overgrowth (MELO) process may not be a commercially viable technique, the results in themselves are significant. Schaub has shown that use of RCE for Si photodiodes can lead to significant leaps in device performance.

To our knowledge there is only one report of purposely-manufactured reflecting Si substrates. Ishikawa et al. [5] used a combination of separation by implantation of oxygen (SIMOX) and MBE to develop a 5-period DBR with a peak reflectance of 90%. Recently, we introduced a Si wafer with a more than 90% reflectance buried DBR for the fabrication of RCE optoelectronic devices [6]. The process uses the Smart-Cut technique for fabricating silicon on insulator (SOI) wafers commercially available from SOITEC SA [7]. Previous x-ray measurements also showed that these reflective SOI wafers were of high crystalline quality. In this paper, we present the responsivity and high-speed measurement results on photodiodes fabricated on these reflecting SOI wafers, showing feasibility of RCE Si detectors for 10 Gb/s optical communication applications at 850 nm.

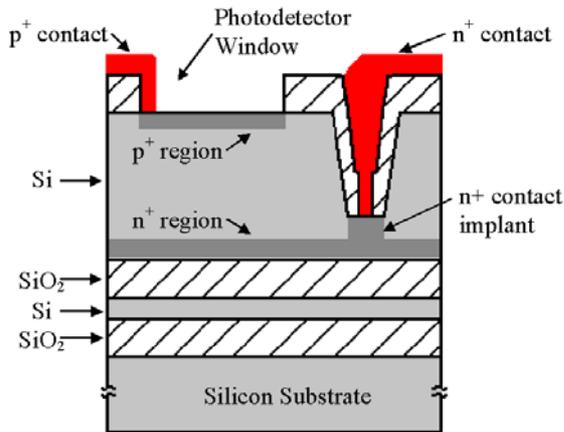


Fig. 2: Cross-section of RCE Si pin photodetector showing trench via for buried n+ contact.

## 2. Photodetector Structure

After the buried DBR fabrication, single crystalline silicon was grown on the double-SOI substrate using a standard low-pressure chemical vapor deposition (LPCVD) epitaxy process. RCE pin photodetectors are fabricated in the epitaxial device layer, which was approximately 2.1 $\mu$ m in total thickness, using standard silicon device fabrication techniques. The structure has a buried n+ implant and a p+ implant on the surface, while the epitaxial silicon layer is left undoped yielding the vertical pin diode. To contact the buried n+ layer a trench was formed using RIE technique with SF<sub>6</sub> reactant and He ambient. A high dose n+ implant was then

performed in the trench to achieve low contact resistance to the n+ silicon. Contacts were formed using Al patterned by a photoresist lift-off technique. The final device structure is shown schematically in Fig. 2.

For on-wafer testing, photodiodes with various dimensions were fabricated with co-planar transmission lines (Fig. 3). The photodiodes were tested for dark current performance as well as spectral quantum efficiency. The dark current density as measured on 200- $\mu$ m-diameter photodiodes varied from 1 to 3  $\mu$ A/cm<sup>2</sup> at reverse bias of 1V to 3V. On 30- $\mu$ m-diameter devices, the dark current is measured as 70 pA to 120 pA at reverse bias of 1V and 3V, respectively. As seen in Fig. 4, the measured spectral quantum efficiency agrees well with the simulation and that the efficiency near 860 nm is approximately 40%, which corresponds to a responsivity of 260 mA/W.

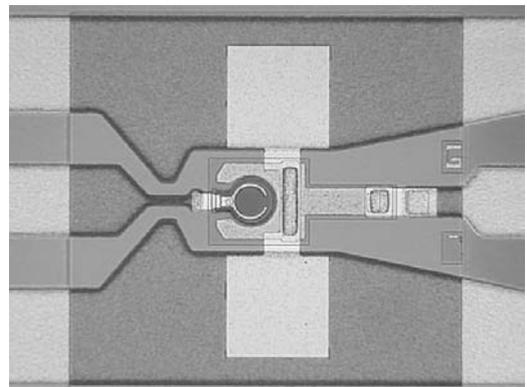


Fig. 3: Top view of finished photodetector showing co-planar transmission lines and coupling capacitors for DC biasing.

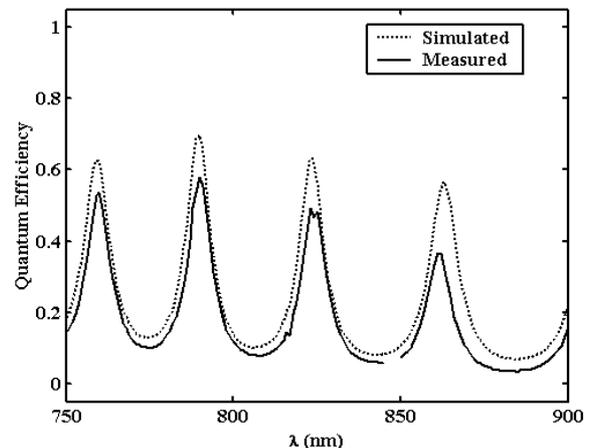


Fig. 4: Spectral quantum efficiency of RCE pin photodetector.

## 3. High-Speed Characterization

High-speed measurements are performed on a micro-wave probe station by using 1.6 ps full-width at half-maximum (FWHM) pulses from a Ti:sapphire laser using a 50 GHz sampling oscilloscope. Figure 5 shows the temporal response obtained at 9 V reverse bias from 30  $\mu$ m- and 100  $\mu$ m-diameter circular devices with respective measured FWHM values of 29 ps and 57 ps. The FWHM of 29 ps suggests a bandwidth well above 10 GHz. However, in these particular devices, a long tail

in the photocurrent response is observed indicative of a diffusion component. To limit the diffusion current due to absorption in doped neutral regions, we have used very thin (less than  $0.2 \mu\text{m}$ ) contact regions. The incomplete depletion of the unintentionally doped absorption region is expected to be the main reason for the diffusion current and resulting reduction in the device speed.

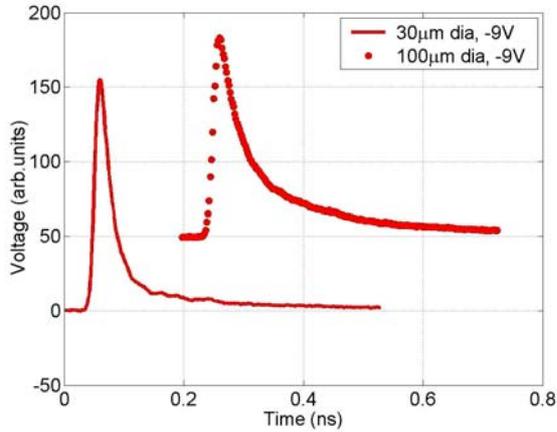


Fig. 5: Measured temporal responses of 30  $\mu\text{m}$ - and 100  $\mu\text{m}$ -diameter photodiodes.

To study the frequency response, measured temporal response data for various size devices at different bias values are converted to frequency domain using fast Fourier transform (FFT). Figure 6 shows the 3 dB bandwidth obtained from a 30  $\mu\text{m}$ -diameter detector under different bias conditions.

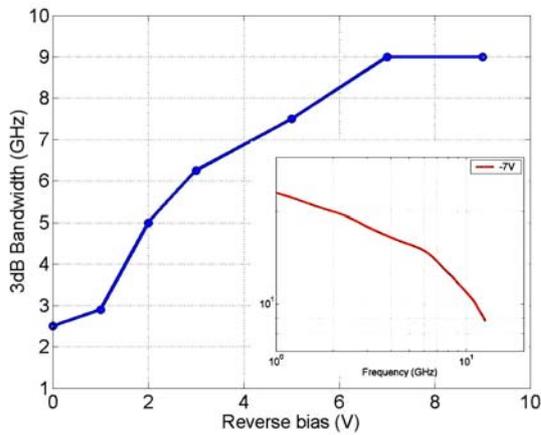


Fig. 6: Frequency bandwidth of 30- $\mu\text{m}$ -diameter device at various bias values calculated from temporal response. The inset shows the Bode plot for 7 V reverse bias.

#### 4. Device Optimization

The benefit of an RCE structure is to increase the efficiency for a given absorption thickness detector while maintaining the bandwidth. Note that the efficiency is an increasing function of the absorption region thickness. Just as increasing the absorption length will increase the efficiency, decreasing the absorption length will increase the bandwidth due to the reduction of carrier transit time. This effect is limited, however, as decreasing the absorption thickness will cause the photodetector

capacitance between the N and P contacts to increase, resulting in the degradation of the device bandwidth. The goal of the designer would be to find the optimal point for absorption length where capacitance and carrier transit time are minimized. The transit time of photodetectors is a function of the device length and the applied bias, as there is a relationship between carrier velocity and applied field. Figure 7 shows the 3 dB bandwidth of a 100  $\mu\text{m}$ -diameter detector with 1.4 V, 3.5 V and 10 V applied reverse bias, for varying absorption lengths.

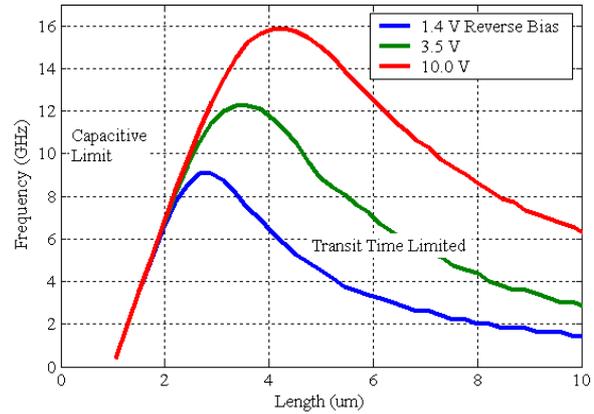


Fig. 7: 3 dB bandwidth of a 100  $\mu\text{m}$ -diameter detector with 1.4 V, 3.5 V and 10 V applied reverse bias.

#### 5. Photodetector Arrays

Several photodetector arrays were fabricated at the EPFL microfabrication facility (CMI) to explore the feasibility of the proposed device structure for multi-channel applications. Figure 8 shows the SEM photograph of the first 7 devices in a 12-device linear array, consisting of 30  $\mu\text{m}$ -diameter detectors placed with a center-to-center separation of 200  $\mu\text{m}$ . It was found that repeatable photodetector characteristics can be achieved in a consistent manner, proving the viability of the proposed RCE photodiode as a versatile building block for high speed optical interfaces.

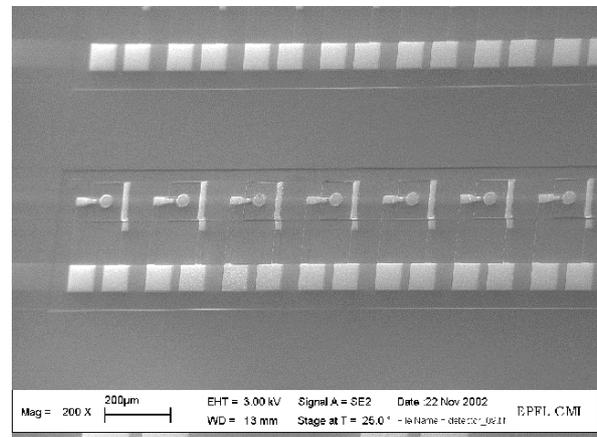


Fig. 8: Partial view of a linear photodetector array consisting of 30  $\mu\text{m}$ -diameter detectors placed with a center-to-center separation of 200  $\mu\text{m}$ .

The electrical performance of the photodetector arrays were tested by using the 12-channel integrated receiver amplifier array HXR2312 by Helix AG. Measurements performed on wire-bonded photodetector arrays have shown that the proposed device structures have performance characteristics that are comparable to commercial devices. The eye diagram pattern obtained at an input signal frequency of 3.0 GHz is seen in Fig. 9.

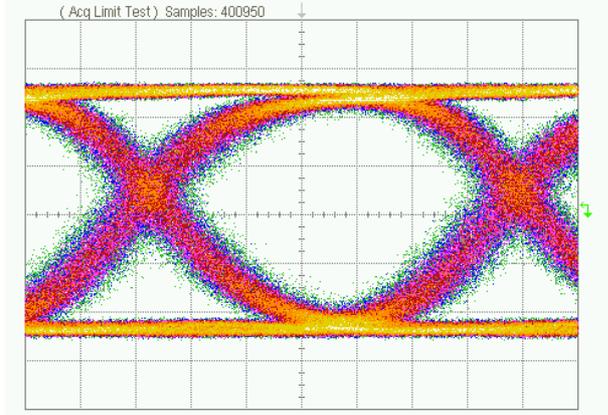


Fig. 9: Eye diagram obtained with HXR2312 12-channel receiver amplifier array at 3.0 GHz.

The measured bit error rate (BER) as a function of input power (in dBm) and for different input signal frequencies is shown in Fig. 10. The reason for the BER curve for 3.0 GHz appearing as shifted to the right was discovered to be due to the 10 nm wavelength mismatch (850 nm vs. 860 nm) between the laser source used in the measurements and the responsivity peak of the photo-detector.

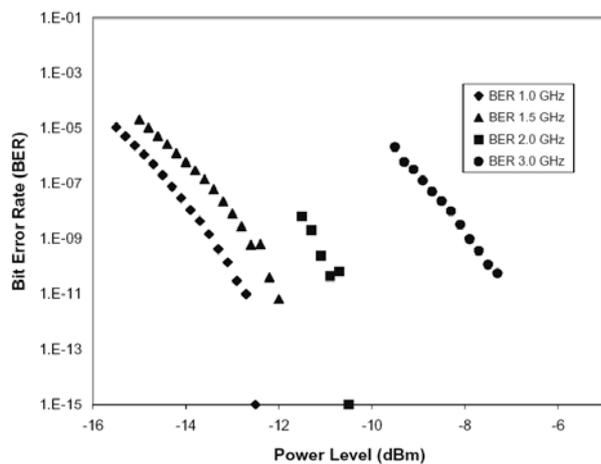


Fig. 10: Bit error rate as a function of the input power, measured at four different input signal frequencies.

## 6. Conclusions

In summary, we present RCE Si pin photodetectors capable of quantum efficiency of ~40% and bandwidth of ~10 GHz at 850 nm with a buried distributed Bragg reflector fabricated by means of a double-SOI technique. The reflecting wafers are commercially reproducible and

have single crystalline silicon device layers for fabricating silicon RCE photodiodes with high bandwidth efficiencies as well as low dark current. These wafers are well suited for VLSI integration and are compatible with standard CMOS processing making them ideal for monolithic integration of receiver circuits with photodetectors. Finally, we demonstrate fully operational linear photodetector arrays with up to 12 devices to prove the feasibility of the proposed device structure for multi-channel applications.

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## References

- [1] M.S. Ünlü, S. Strite, *Applied Physics Reviews*, vol. 78, no. 2, pp. 607-638, (1995).
- [2] J.C. Campbell, *Proceedings of IEEE International Electron Devices Meeting*, Washington, DC, 10-13 December 1995, pp. 575-578.
- [3] J. C. Bean, et al., *IEEE Photonics Technology Letters*, vol. 9, no. 6, pp. 806-808, (1997).
- [4] J.D. Schaub, R. Li, C.L. Schow, J.C. Campbell, *IEEE Photonics Technology Letters*, vol. 11, no. 12, pp. 1647-1649, (1999).
- [5] Y. Ishikawa, N. Shibata, S. Fukatsu, *Applied Physics Letters*, vol. 69, no. 25, pp. 3881-3883, (1996).
- [6] M. K. Emsley and M. S. Ünlü, *Proceedings of IEEE Lasers and Electro-Optics Society 2000 Annual Meeting*, Rio Grande, Puerto Rico, 13-16 November 2000, vol. 2, pp. 432-433.
- [7] M. Bruel, *Electronics Letters*, vol.31, no.14, pp.1201-1202, (1995).