Epitaxy-Ready Reflecting Substrates for Resonant-Cavity-Enhanced Silicon Photodetectors

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Resonant cavity enhanced (RCE) photodetectors have been the focus of extensive research over the past decade in the design of high bandwidth-efficiency product devices [1]. The quantum efficiency η of conventional detectors is governed by the optical absorption of the semiconductor material. For semiconductors with low absorption coefficients, thick absorption regions are required to achieve high η limiting the bandwidth of photodetectors. Silicon-based photodetectors for applications in optical communications in the near-IR wavelength range between 800-900 nm suffer from low bandwidth-efficiency products due to the long absorption length necessitated by the small absorption coefficient. Increasing the bandwidth-efficiency product is the inherent benefit of a RCE structure, which relies on the constructive interference of a Fabry-Perot cavity to enhance the optical field inside the photodetector at specific wavelengths. For semiconductor photodetectors, such a resonant cavity can be formed using a buried reflector and the air/semiconductor top interface. The buried reflector is typically formed by alternating layers of semiconductors with different refractive indices. Due to the availability of heterostructures compound semiconductors have been the focus of RCE photodetector development [1]. Formation of buried mirrors and resonant cavities have remained as a challenge in Si technology.

Numerous attempts have been made to fabricate silicon RCE photodetectors [2], [3]. Earlier devices utilized Si device structures deposited on top of dielectric mirrors. Various attempts included CVD as well as MBE [4], which resulted in a polycrystalline silicon device layer. Photodiodes fabricated on this device layer typically suffered from high dark currents. Schaub, et al. [5], has reported silicon RCE photodiodes with low dark currents that achieved a bandwidth in excess of 34 GHz – the highest speed recorded for Si p-i-n photodiodes. These RCE structures used a merged epitaxial layer overgrowth (MELO) process to form the absorption region on top of the buried distributed Bragg reflector (DBR). Although this growth process is not a commercially viable technique the results in themselves are significant, Schaub has shown that use of RCE for silicon photodiodes can lead to significant leaps in device performance.

To the author's knowledge only one report has been written on purposely-manufactured reflecting substrates. Ishikawa et al. [6] used a combination of separation by implantation of oxygen (SIMOX) and epitaxy to develop a DBR with a peak reflectance of 90%. The DBR used 5 periods of Si/SiO_2 which were created using SIMOX to produce the buried oxide layer and molecular beam epitaxy (MBE) to grow the silicon layers. Their work showed that the choice of layer thickness for SiO_2 and Si was limited to a SiO_2/Si thickness ratio of less than unity due to poor interface morphology. This result is a critical limitation as in an optimally tuned structure the optical path lengths in SiO_2 and Si are identical, which means the layer thickness of SiO_2 is larger than that of Si since SiO_2 has a smaller refractive index. This means that the SiO_2/Si width ratio is greater than unity for an optimally tuned structure. They were able to produce highly reflective dielectric mirrors only after 10 layers were grown. Another draw back of their technique is that it utilized a complex in-situ implantation and epitaxy process that required specialized equipment.

We introduce a commercially reproducible silicon wafer with a buried DBR for silicon RCE photodiodes. These wafers have a high reflectance and are device grade wafers for electrical circuit fabrication. Through proprietary fabrication techniques silicon wafers were manufactured with wavelength optimized buried DBR structures with reflectivity in excess of 90% using only a 2 period Si/SiO_2 structure. The wafers have an epitaxy ready single crystalline surface. A cross-sectional SEM of the 2 period DBR is shown in Fig. 1.

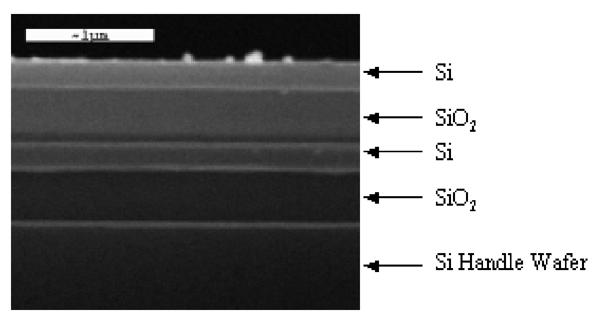

Fig. 1. Cross-sectional SEM of reflecting silicon substrate showing buried distributed Bragg reflector.

Crystalline quality characterization was performed using a Rigaku rotating anode x-ray machine and four-circle diffractometer to perform rocking curve analysis. In order to extract the crystalline quality of the surface layer, and to decouple the underlying silicon substrate, a grazing incidence x-ray scan was employed. Measurements of the surface silicon device layer revealed a 0.16648° rocking curve width. This compares with a 0.16060° rocking curve width for a reference standard silicon wafer. This measurement showed that within the experimental resolution the two wafers were identical in crystalline quality.

The substrate's reflectivity was specifically tuned to achieve a high reflectance at 850 nm for short haul optical communication systems. The reflectivity of this structure is seen in Fig. 2.

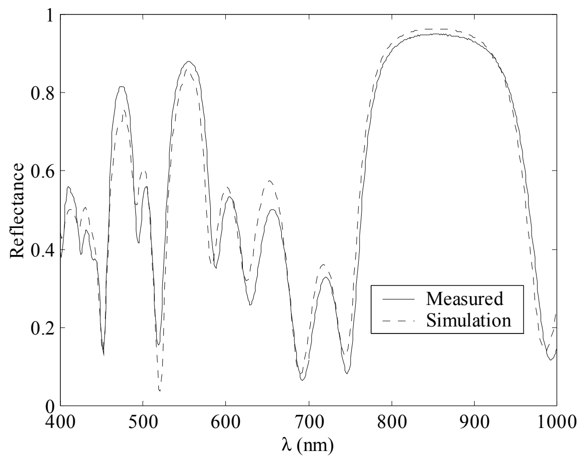

Fig. 2. Reflectivity of two period distributed bragg reflector showing excellent fit with simulated results.

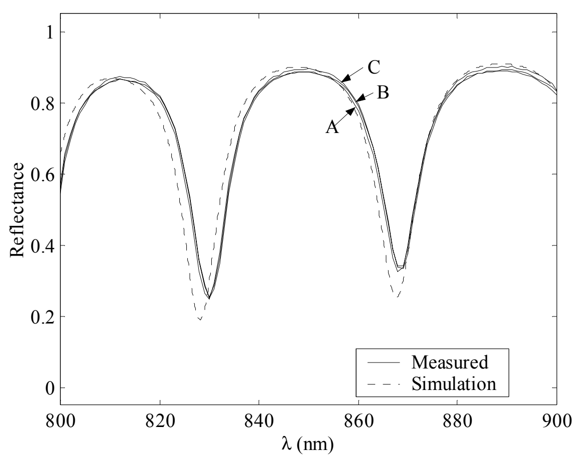

Fig. 3. Reflectivity of final silicon wafer (acquired at three random locations on wafer) with buried distributed Bragg reflector.

After the buried DBR fabrication, single crystalline silicon was grown on the silicon surface using a standard LPCVD epitaxy process. The surface silicon layer was grown to approximately 2.1μm in total thickness. The resulting structure has a reflectivity shown in Fig. 3. It can be seen in Fig. 3 that reflectivity is reduced to less then 40% which could yield predicted photodiode quantum efficiencies in excess of 50%.

It can also be seen in Fig. 3 that the minimum reflectivity, or maximum quantum efficiency, for photodiodes manufactured on these wafers would not be at the desired 850 nm wavelength. Even the strictest control over the manufacturing process will leave inconsistencies in the layer thickness desired for optimal results. It is therefore imperative that a technique be available for spectrally tuning the silicon wafers. We will show that through the use of surface recessing via silicon etching, spectral tuning of the reflectance minimum can be achieved. Fig. 4 shows the simulated results of spectral tuning on the reflecting silicon substrates through the recessing of the silicon surface.

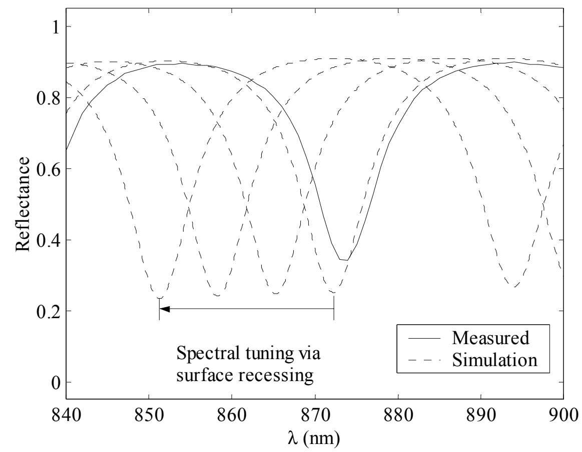

Fig. 4. Simulated effect of surface recessing for use in spectral tuning of the reflectance minima.

We have presented a commercially reproducible single crystalline silicon wafer with a buried distributed Bragg reflector. These wafers can be used for fabricating silicon RCE photodiodes with high bandwidth efficiencies as well as low dark current.

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