High-Speed Resonant-Cavity-Enhanced Silicon Photodetectors on Reflecting Silicon-On-Insulator Substrates

Matthew K. Emsley, Olufemi Dosunmu, and M. Selim Ünlü

***Abstract*—In this letter, we report a resonant-cavity-enhanced Si photodetector fabricated on a reflecting silicon-on-insulator (SOI) substrate. The substrate incorporates a two period distributed Bragg reflector (DBR) fabricated using a commercially available double-SOI process. The buried DBR provides a 90% reflecting surface. The resonant-cavity-enhanced Si photodetectors have 40% quantum efficiency at 860 nm and response time of 29 ps. These devices are suitable for 10-Gb/s data communications.**

***Index Terms*—Photodetector, resonant cavity enhanced, silicon, silicon on insulator.**

I. Introduction

RESONANT-CAVITY-ENHANCED (RCE) photodetectors have been the focus of extensive research over the past decade in the design of high bandwidth-efficiency product devices [1]. The quantum efficiency η of conventional detectors is governed by the optical absorption of the semiconductor material. For semiconductors with low absorption coefficients, thick absorption regions are required to achieve high η, limiting the bandwidth of photodetectors. Silicon-based photodetectors for applications in optical communications in the near-IR wavelength range between 800–900 nm suffer from low bandwidth-efficiency products due to the long absorption length necessitated by the small absorption coefficient. Increasing the bandwidth-efficiency product is the inherent benefit of a RCE structure, which relies on the constructive interference of a Fabry–Pérot cavity to enhance the optical field inside the photodetector at specific wavelengths. For semiconductor photodetectors, such a resonant cavity can be formed using a buried reflector and the air/semiconductor top interface. Alternating layers of semiconductors with different refractive indices are used to fabricate the buried reflector. Due to the availability of heterostructures, compound semiconductors have been the focus of RCE photodetector development [1]. Formation of buried mirrors and resonant cavities have remained as a challenge in Si technology.

Several attempts have been made to fabricate silicon RCE photodetectors [2], [3]. Earlier devices utilized Si device structures deposited on top of dielectric mirrors. Various attempts included chemical vapor deposition (CVD), as well as molecular beam epitaxy (MBE) [4], which resulted in a polycrystalline silicon device layer, due to the amorphous seed layer. Photodiodes fabricated on a polycrystalline device layer typically suffered from high dark currents. Schaub *et al.* [5], has reported silicon RCE photodiodes with low dark currents that achieved a bandwidth in excess of 34 GHz—the highest speed recorded for Si pin photodiodes. These RCE structures used a merged epitaxial layer overgrowth (MELO) process to form the absorption region on top of the buried distributed Bragg reflector (DBR). Although this growth process would be difficult to reproduce commercially, the results in themselves are significant. Schaub *et al.* has shown that use of RCE for silicon photodiodes can lead to significant leaps in device performance.

To our knowledge, there is only one report of purposely manufactured reflecting Si substrates. Ishikawa *et al.* [6] used a combination of separation by implantation of oxygen (SIMOX) and epitaxy to develop a DBR with a peak reflectance of 90%. The DBR used five periods of Si–SiO_2 which were created using SIMOX to produce the buried oxide layer and molecular beam epitaxy (MBE) to grow the silicon layers. Their work showed that the choice of layer thickness for SiO_2 and Si was limited to a SiO_2–Si thickness ratio of less than unity due to poor interface morphology. This result is a critical limitation as in optimally tuned structures the optical path lengths in SiO_2 and Si are identical, which means the layer thickness ratio of SiO_2–Si is approximately 2.5. They were able to produce highly reflective dielectric mirrors only after ten layers were grown. Another drawback of their technique is that it utilized a complex insitu implantation and epitaxy process that required specialized equipment. We have introduced a silicon wafer with a high reflectance buried DBR for the fabrication of RCE optoelectronic devices [7]. These substrates, manufactured by a repeated silicon-on-insulator (SOI) process, are device grade quality for electrical circuit fabrication. In this letter, we report high-speed and high-efficiency RCE Si pin photodetectors fabricated on these high reflectivity double-SOI wafers.

II. Wafer and Device Fabrication

Silicon wafers were manufactured with buried DBR structures having a reflectivity in excess of 90% using only a two period Si–SiO_2 structure. The process uses the smart-cut technique for fabricating SOI wafers commercially available from SOITEC SA [8]. Oxidized silicon wafers are implanted with hydrogen ions and then brought into contact with a second silicon

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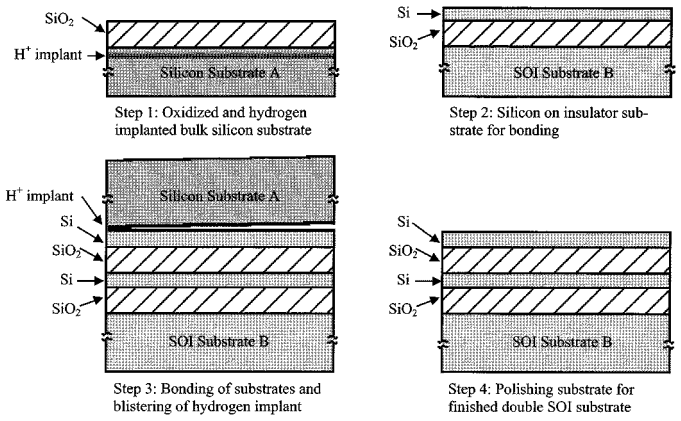

Fig. 1. Double-SOI fabrication process showing wafer bonding and substrate separation.

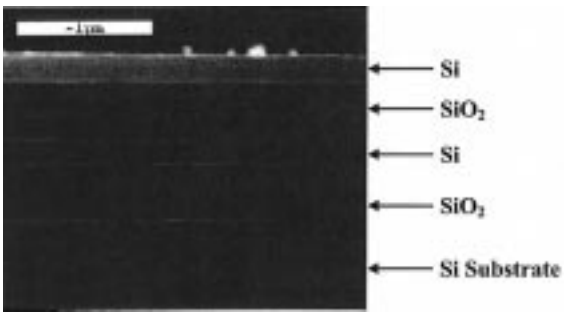

Fig. 2. Cross-sectional SEM of reflecting silicon substrate showing buried DBR.

wafer to form a hydrophilic bond. The bonded wafers undergo a two-phase heat treatment, which first splits the wafers into two parts at the hydrogen implant depth at a low temperature, the result being a transfer of a thin silicon region onto the oxidized silicon wafer, and second a high temperature treatment of the SOI wafer to strengthen the bond. This process yields a single SOI wafer. Performing this process a second time, with the exception of bonding the hydrogen implanted oxidized wafer to the SOI wafer instead of a bulk silicon wafer, yields a double-SOI structure. The second phase of this process is illustrated in Fig. 1. The wafers have an epitaxy ready single crystalline surface. A cross-sectional SEM of the double-SOI substrate is shown in Fig. 2.

Characterization of crystalline quality was performed using a Rigaku rotating anode X-ray machine and four-circle diffractometer to perform rocking curve analysis. In order to extract the crystalline quality of the surface layer, and to decouple the underlying silicon substrate, a grazing incidence X-ray scan was employed. Measurements of the surface silicon device layer revealed a 0.1665° rocking curve width. This compares with a 0.1606° rocking curve width for a reference standard silicon wafer. This measurement showed that within the experimental resolution the two wafers were identical in crystalline quality.

The substrate's layer structure was chosen to achieve a high reflectance at 850 nm for short haul optical communication systems. Fig. 3 shows the substrate's reflectivity and its close agreement with the predicted value. It should be noted that the simulation was fitted to the measured value by manipulating the

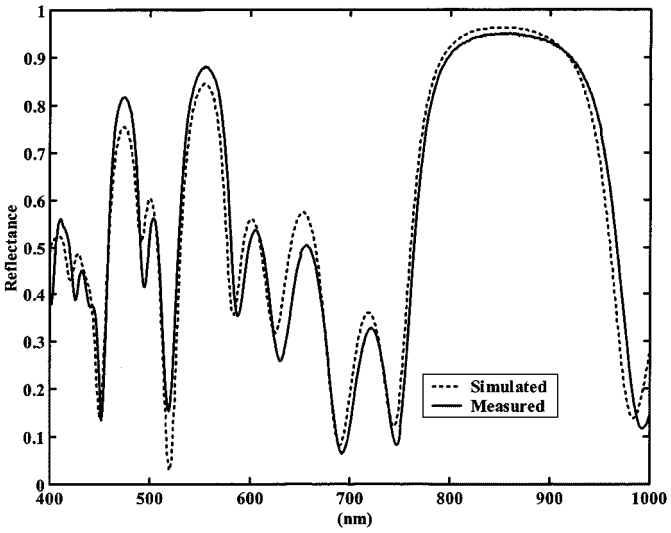

Fig. 3. Reflectivity of two period DBR showing excellent fit with simulated results.

layer thickness of the DBR structure. The double-SOI fabrication scheme had a 10% tolerance on layer thickness, but through the data fitting it was shown that the layers were within 7% of the desired thickness.

After the buried DBR fabrication, single crystalline silicon was grown on the double-SOI substrate using a standard low-pressure chemical vapor deposition (LPCVD) epitaxy process. Resonant-cavity-enhanced pin photodetectors were fabicated in the epitaxial device layer, which was approximately 2.1 μm in total thickness, using standard silicon device fabrication techniques. The structure had a buried n+ implant and a p+ implant on the surface, while the epitaxial silicon layer is left undoped yielding the vertical pin diode. To contact the buried n+ layer a trench was formed using RIE technique with SF6 reactant and He ambient. A high dose n+ implant was then performed in the trench to achieve low contact resistance to the n+ silicon. Contacts were formed using Al patterned by a photoresist liftoff technique. For on-wafer high-speed testing, photodiodes with various dimensions were fabricated with coplanar transmission lines. The final device structure is shown schematically in Fig. 4.

III. Results and Discussion

The photodetectors were tested for dark current performance, as well as spectral quantum efficiency. The dark current as measured on 200-μm-diameter photodetectors varied from 1 to 3 μA/cm^2 at reverse bias of 1 to 3 V. On 30-μm-diameter devices, the dark current was measured as 70 to 120 pA at a reverse bias of 1 and 3 V, respectively.

Spectral quantum efficiency measurements were performed using a variable wavelength Ti–Sapphire laser source, lock-in amplifier, and a reference silicon photodetector with known spectral responsivity for photocurrent normalization. It can be seen from Fig. 5 that the spectral quantum efficiency agrees well with the simulation and that the efficiency near 860 nm is approximately 40%, which corresponds to a responsivity of 260 mA/W.

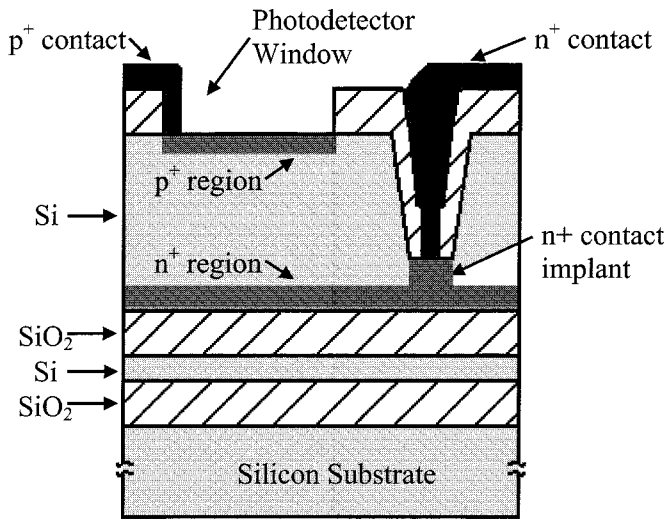

Fig. 4. Cross section of RCE Si pin photodetector showing trench via for buried n+ contact.

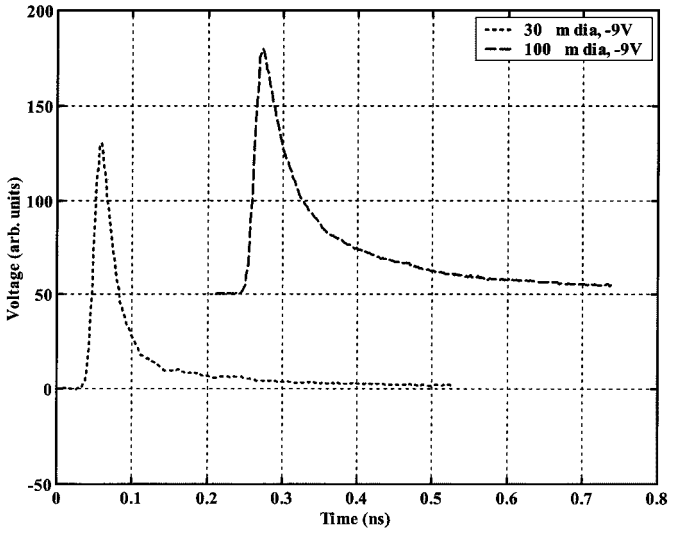

Fig. 6. Measured temporal responses of 30- and 100-μm-diameter photodiodes.

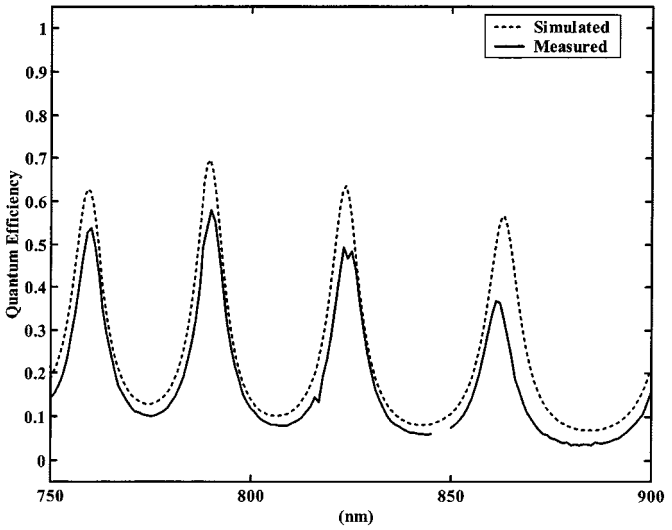

Fig. 5. Spectral quantum efficiency of RCE pin photodetector.

High-speed measurements are performed on a microwave probe station using a 50-GHz sampling oscilloscope on the photodetector response to 1.6 ps full-width at half-maximum (FWHM) pulses from a Ti:sapphire laser source. Fig. 6 shows the temporal response obtained at 9 V reverse bias from 30-μm and 100-μm-diameter circular devices with respective measured FWHM values of 29 and 57 ps. The FWHM of 29 ps suggests a bandwidth above 10 GHz, which is well beyond the requirements for 10-Gb/s data communications.

IV. Conclusion

We presented RCE Si pin photodetectors capable of quantum efficiencies above 40% at 850 nm and response times of 29 ps with a buried distributed Bragg reflector fabricated by means of a double-SOI technique. The reflecting wafers are commercially reproducible and have single crystalline silicon device layers for fabricating silicon RCE photodiodes with high bandwidth efficiencies as well as low dark current. These wafers are well suited for VLSI integration and are compatible with standard CMOS processing making them ideal for monolithic integration of receiver circuits with photodetectors.

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References

[1] M. S. Ünlü and S. Strite, "Resonant cavity enhanced photonic devices," *Appl. Phys. Rev.*, vol. 78, no. 2, pp. 607–638, 1995.

[2] J. C. Campbell, "Resonant-cavity photodiodes," in *Proc. IEEE Int. Electron Devices Meeting*, Washington, DC, Dec. 10–13, 1995, pp. 575–578.

[3] D. C. Diaz, C. L. Schow, J. Qi, and J. C. Campbell, "Si/SiO_2 resonant cavity photodetector," *Appl. Phys. Lett.*, vol. 69, no. 19, pp. 2798–2800, 1996.

[4] J. C. Bean, J. Qi, C. L. Schow, R. Li, H. Nie, J. Schaub, and J. C. Campbell, "High speed polysilicon resonant-cavity photodiode with SiO_2/Si Bragg reflectors," *IEEE Photon. Technol. Letters*, vol. 9, pp. 806–808, June 1997.

[5] J. D. Schuab, R. Li, C. L. Schow, and J. C. Campbell, "Resonant-cavity-enhanced high-speed Si photodiode grown by epitaxial lateral overgrowth," *IEEE Photon. Technol. Lett.*, vol. 11, pp. 1647–1649, Dec. 1999.

[6] Y. Ishikawa, N. Shibata, and S. Fukatsu, "Epitaxy-ready Si/SiO_2 Bragg reflectors by multiple separation-by-implanted-oxygen," *Appl. Phys. Lett.*, vol. 69, no. 25, pp. 3881–3883, 1996.

[7] M. K. Emsley and M. S. Ünlü, "Epitaxy-ready reflecting substrates for resonant-cavity-enhanced silicon photodetectors," in *Proc. IEEE Lasers and Electro-Optics Society 2000 Annual Meeting*, vol. 2, Rio Grande, Puerto Rico, Nov. 13–16, 2000, pp. 432–433.

[8] M. Bruel, "Silicon on insulator material technology," *Electron. Lett.*, vol. 31, no. 14, pp. 1201–1202, 1995.