

# Transient Simulation of Heterojunction Photodiodes—Part I: Computational Methods

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**Abstract**—A novel approach is presented for incorporating the transient solution of one-dimensional semiconductor drift-diffusion equations within a general circuit simulation tool. This approach allows simple representation of localized carrier transport models of simulated devices through equivalent circuit elements such as voltage controlled current sources and capacitors. It also lends itself to mixed-mode transient simulation of devices and circuits. The utility of the new simulation approach in state-of-the-art device design is demonstrated by the transient response analysis of a GaAs heterojunction  $p-i-n$  photodiode, and by the time-domain analysis of an integrated photoreceiver circuit.

## I. INTRODUCTION

ACCURATE SIMULATION of transient electrical behavior of optoelectronic devices under realistic operating conditions is becoming an increasingly important concern in OEIC (Optoelectronic Integrated Circuit) design and optimization. Device-level simulation of novel structures ideally allows the detailed investigation and analysis of complex phenomena that cannot be achieved through experiments or through simple analytic models. It also provides valuable insight into the physical mechanisms which ultimately determine the operational performance of the device. A number of semiconductor device simulation tools have been developed over the years [1]–[3], and are being widely used for device development tasks. Most of the existing device simulators are based on the drift-diffusion (DD) description of carrier transport, and employ specialized techniques to obtain the one-, two-, or three-dimensional solutions in time domain.

The simulation of optoelectronic devices, however, presents some specific challenges that are not well addressed by the existing device simulation tools. One important requirement is that the local absorption and photo-generation (light-induced carrier generation) effects should be explicitly representable at any point within the device. The simulation tool should enable

Manuscript received June 21, 1993, revised November 27, 1994. This work was supported by the National Science Foundation under Grant ECS-9309607.

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IEEE Log Number 9409164.

simple modeling of photodetectors which has localized optical absorption in specific regions, and should be capable of fast transient response simulation. Besides, the tools should allow simple integration of circuit-level and device-level simulation tasks, especially for the analysis of integrated circuit response under various conditions. Finally, simple extraction of device and circuit model parameters is desirable, to aid the development of compact simulation models for novel optoelectronic devices.

The advantages of mixed device/circuit simulation capability are quite obvious. There exists a growing consensus that process, device and circuit simulation tools used as separate entities need to be integrated into a combined simulation environment for efficient design and optimization of semiconductor devices and integrated circuits. Such integration will shorten the development cycle for new technologies by providing accurate predictions of various physical phenomena on the device and circuit level and by allowing the investigation of detailed device behavior within the circuit environment. The majority of the proposed tool integration approaches seek either to create specific mixed-mode simulation environments [4]–[6], or to combine specialized device and circuit simulation tools through user-friendly interfacing environments [7], [8].

In this paper, a novel approach is presented for incorporating the transient solution of one-dimensional semiconductor drift-diffusion equations *within a general circuit simulation tool*, which eliminates the need of interfacing various device and circuit simulation environments. This approach allows for the simple representation of localized carrier transport models of simulated devices using equivalent circuit elements such as voltage-controlled current sources and capacitors. The availability of local photo-generation models at every grid point enables accurate transient simulation of various optoelectronic devices, without any restrictions on light absorption and carrier generation characteristics. The approach is conceptually simple and very easy to implement in many existing circuit simulation environments, with only moderate amount of additional effort. Besides the inherent advantage of providing mixed-mode device and circuit simulation capability embedded in a circuit simulator, this approach can also be used for extracting the device- and circuit-level model parameters to match measured data through optimization.

In the following two sections, the discretization of the time-dependent semiconductor equations, a detailed derivation of model parameters, and the implementation of the

drift-diffusion model using equivalent circuit elements are presented. The application of the new approach is discussed in Section IV with several device and mixed mode device/circuit simulation examples.

## II. DISCRETIZATION OF SEMICONDUCTOR EQUATIONS

Carrier transport in semiconductors is described by three coupled partial differential equations, namely, the Poisson's equation, the electron-current continuity equation and the hole-current continuity equation. Assuming that the carrier flow and the potential distribution within a semiconductor structure are confined to one dimension ( $x$ ), the normalized carrier transport equations are given as follows.

$$\frac{\partial^2 V}{\partial x^2} - \frac{1}{r} [n - p + N_A - N_D] = 0 \quad (1)$$

$$\frac{\partial n}{\partial t} = \frac{1}{q} \frac{\partial J_n}{\partial x} - R_n + G_n \quad (2)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \frac{\partial J_p}{\partial x} - R_p + G_p \quad (3)$$

The electron and hole current densities  $J_n$  and  $J_p$  are defined as

$$J_n = \mu_n \frac{\partial n}{\partial x} - n \mu_n \frac{\partial (V + V_n)}{\partial x} \quad (4)$$

$$J_p = -\mu_p \frac{\partial p}{\partial x} - p \mu_p \frac{\partial (V - V_p)}{\partial x} \quad (5)$$

Here, the normalized variables  $V$ ,  $n$  and  $p$  represent the local electrostatic potential, the electron concentration and the hole concentration, respectively. The parameter  $r$  represents the normalized dielectric constant,  $R$  and  $G$  represent carrier recombination and generation rates, respectively. Two potentials  $V_n$  and  $V_p$  are also introduced as band parameters to account for the bandgap variations in heterostructures, and are defined as follows,

$$qV_n = \chi - \chi_r + kT \ln \left( \frac{N_C}{N_{Cr}} \right) \quad (6)$$

$$qV_p = -\left[ \chi - \chi_r + E_G - E_{Gr} - kT \ln \left( \frac{N_V}{N_{Vr}} \right) \right] \quad (7)$$

where  $N_C$  and  $N_V$  are density of states for conduction and valence bands, respectively,  $\chi$  is the electron affinity, and subscript  $r$  denotes the reference material.

To obtain the solution of the semiconductor equations (1)–(3) by using the finite difference method, the equations need to be discretized on a nonuniform one-dimensional grid (Fig. 1). Usually, the discretization of the time-dependent semiconductor equations is carried out both in time-domain and in space-domain [10]. In the following, the dependent variables will be discretized with respect to the space (position) variable  $x$ , but they will be left continuous in time, resulting in a semi-discrete form. The goal of this formulation is to facilitate a simple implementation of the device model within

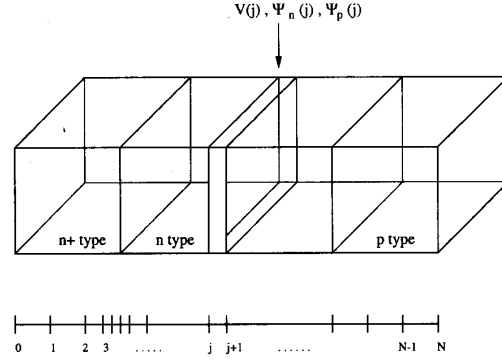


Fig. 1. Partitioning of a  $p-n-n^+$  structure on a one-dimensional nonuniform grid.

the circuit simulation environment. Three new local variables are defined as  $x_1(j) = V(j)$ ,  $x_2(j) = V(j) - \psi_n(j)$ , and  $x_3(j) = -V(j) + \psi_p(j)$  where the normalized variables  $V$ ,  $\psi_n$ , and  $\psi_p$  represent the local electrostatic potential, the electron and hole quasi-Fermi potentials, respectively. The Scharfetter–Gummel approximation has been used to express the current densities  $J_n$  and  $J_p$  in terms of the carrier concentrations [9]:

$$J_n(j + \frac{1}{2}) = \frac{\mu_{n(j+\frac{1}{2})} \Delta_n(j)}{h_{j+1}} \left[ \frac{n(j+1) \exp(\Delta_n(j)) - n(j)}{\exp(\Delta_n(j)) - 1} \right] \quad (8)$$

$$J_p(j + \frac{1}{2}) = -\frac{\mu_{p(j+\frac{1}{2})} \Delta_p(j)}{h_{j+1}} \left[ \frac{p(j+1) \exp(\Delta_p(j)) - p(j)}{\exp(\Delta_p(j)) - 1} \right] \quad (9)$$

where

$$\Delta_n(j) = V(j) + V_n(j) - V(j+1) - V_n(j+1) \quad (10)$$

$$\Delta_p(j) = V(j+1) - V_p(j+1) - V(j) - V_p(j) \quad (11)$$

The carrier concentrations,  $n$  and  $p$ , are related to the local potential variables as

$$\begin{aligned} n(j) &= \exp [V(j) + V_n(j) - \psi_n(j)] \\ &= \exp [x_2(j) + V_n(j)] \end{aligned} \quad (12)$$

$$\begin{aligned} p(j) &= \exp [-V(j) + V_p(j) + \psi_p(j)] \\ &= \exp [x_3(j) + V_p(j)]. \end{aligned} \quad (13)$$

Substituting (8)–(11) into the device equations (1)–(3), a set of time-dependent space-discretized equations are obtained on a nonuniform one-dimensional grid.

Here, (14), shown at the bottom of the next page, corresponds to the discretized Poisson's equation at the  $j$ th grid node, and (15) and (16), also shown at the bottom of the next page, correspond to the electron continuity and hole continuity equations, respectively. In (14)–(16), the variation of electron and hole mobilities as a function of doping and local electric

field is being taken into account by a suitable local mobility model based on carrier velocity saturation. The introduction of band gap parameters  $V_n$  and  $V_p$  allows simple representation of the band gap variation effects in heterostructures [16]. Notice that a photon-induced carrier generation term  $G_j$  is available at every grid point  $x_j$ , and it can be represented by an independent current source. The extension of this approach for two-dimensional semiconductor equations is also straightforward. Assuming a rectangular space-grid structure, the Poisson's equation, the electron continuity equation, and the hole continuity equation can easily be discretized at each grid point. In this case, each discretized equation contains the electrostatic potential and Fermi potential variables of the four (instead of two) neighboring grid points, as well as those of the grid point itself. Thus the resulting set of time-continuous and space-discretized equations will again be characterized by next-neighbor relations in the space domain.

The carrier generation/recombination rate at any grid point is assumed to be a function of two basic mechanisms, i.e., trap-related phonon transitions and photon transitions. The four partial processes involved in phonon transitions are: 1) electron capture from the conduction band by an unoccupied trap, 2) hole capture i.e., release of an electron from an occupied trap to the valence band, 3) electron emission from an occupied trap to the conduction band, and 4) hole emission, i.e., electron capture from the valence band by an unoccupied trap. The well-known Shockley-Read-Hall model accounts for the total generation/recombination rate due to phonon transitions listed above [10].

$$R_j = \frac{n(j)p(j) - 1}{\tau_p(n(j) + n_1) + \tau_n(p(j) + p_1)} \quad (17)$$

where  $n(j)$  and  $p(j)$  represent the electron and hole concentrations at the  $j$ th grid point, and  $\tau_n$  and  $\tau_p$  represent the carrier lifetimes.

The photon transitions on the other hand, are assumed to be exclusively in the form of optical *generation* of carriers, described as an electron gaining energy from incident photons and moving from the valence band to the conduction band. This process is represented by the photon-induced carrier generation term  $G_j$  at each grid point.

Next, the time-domain solution of these discretized drift-diffusion equations will be examined in detail.

### III. IMPLEMENTATION OF THE MODEL

The semi-discrete carrier transport equations (14)–(16) describe the transient behavior of the electrostatic potential and the Fermi potentials at any grid point. Using the Shockley-Read-Hall generation/recombination model,  $R_j$  can also be expressed in terms of electrostatic potential and the Fermi potentials at the  $j$ th grid point, as follows [10], [11]

$$R_j = \frac{\exp(x_2 + V_n) \exp(x_3 + V_p) - 1}{\tau_p(\exp(x_2 + V_n) + n_1) + \tau_n(\exp(x_3 + V_p) + p_1)} \quad (18)$$

Thus, (8)–(10) assume the following general form.

$$x_1(j) = f_1[x_1(j+1), x_1(j-1), x_2(j), x_3(j), V_n(j), V_p(j)]. \quad (19)$$

It is seen that the electrostatic and Fermi potentials at any grid point are described by three coupled nonlinear differential equations in time domain which involve the corresponding potential variables as well as the neighboring grid node potentials. With a simple variable assignment, the (19)–(21) can be

$$x_1(j) = \frac{h_j h_{j+1}}{r_{j+\frac{1}{2}} h_j + r_{j-\frac{1}{2}} h_{j+1}} \times \frac{h_j + h_{j+1}}{2} \times \left[ \exp(x_3(j) + V_p(j)) - \exp(x_2(j) + V_n(j)) + C_j \right] + \frac{r_{j+\frac{1}{2}} h_j x_1(j+1) + r_{j-\frac{1}{2}} h_{j+1} x_1(j-1)}{r_{j+\frac{1}{2}} h_j + r_{j-\frac{1}{2}} h_{j+1}} \quad (14)$$

$$\frac{\partial x_2(j)}{\partial t} = \frac{2\mu_n(j+\frac{1}{2})}{(h_j + h_{j+1})h_{j+1}} [x_1(j) - x_1(j+1) + V_n(j) - V_n(j+1)] \left\{ \frac{\exp[x_2(j+1) - x_2(j) + x_1(j) - x_1(j+1)] - 1}{\exp[x_1(j) - x_1(j+1) + V_n(j) - V_n(j+1)] - 1} \right\} + \frac{2\mu_n(j-\frac{1}{2})}{(h_j + h_{j+1})h_j} [x_1(j) - x_1(j-1) + V_n(j) - V_n(j-1)] \left\{ \frac{\exp[x_2(j-1) - x_2(j) + x_1(j) - x_1(j-1)] - 1}{\exp[x_1(j) - x_1(j-1) + V_n(j) - V_n(j-1)] - 1} \right\} - \frac{R_j - G_j}{\exp(x_2(j) + V_n(j))} \quad (15)$$

$$\frac{\partial x_3(j)}{\partial t} = \frac{2\mu_p(j+\frac{1}{2})}{(h_j + h_{j+1})h_{j+1}} [x_1(j) - x_1(j+1) + V_p(j) - V_p(j+1)] \left\{ \frac{\exp[x_3(j+1) - x_3(j) + x_1(j+1) - x_1(j)] - 1}{\exp[x_1(j+1) - x_1(j) + V_p(j) - V_p(j+1)] - 1} \right\} + \frac{2\mu_p(j-\frac{1}{2})}{(h_j + h_{j+1})h_j} [x_1(j-1) - x_1(j) + V_p(j) - V_p(j-1)] \left\{ \frac{\exp[x_3(j-1) - x_3(j) + x_1(j-1) - x_1(j)] - 1}{\exp[x_1(j-1) - x_1(j) + V_p(j) - V_p(j-1)] - 1} \right\} - \frac{R_j - G_j}{\exp(x_3(j) + V_p(j))} \quad (16)$$

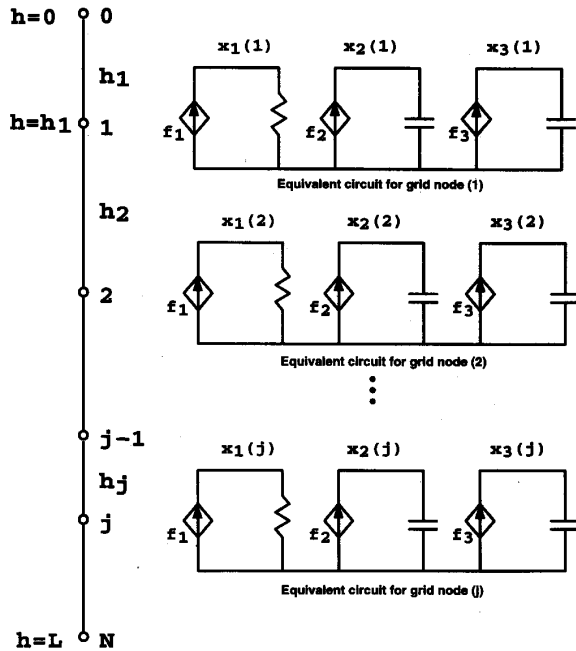


Fig. 2. The one-dimensional finite difference grid and the equivalent-circuit representation of the variables associated with each grid point.

represented by an equivalent circuit, which can then be solved using a conventional transient circuit simulation program such as SPICE. For a simple equivalent circuit interpretation of these equations, first let the variables  $x_1$ ,  $x_2$  and  $x_3$  represent three node voltages. Also, let the right-hand sides of (19)–(21), i.e., the functions  $f_1$ ,  $f_2$  and  $f_3$  represent the currents of three nonlinear voltage-controlled current sources. Then, (20) and (21), shown at the bottom of the page, can be interpreted as the state equations of linear capacitors with terminal currents of  $f_2$  and  $f_3$ , respectively, while equation (19) describes the terminal voltage of a unit resistor with a terminal current of  $f_1$ . The equivalent circuit diagrams corresponding to (19)–(21) are given in Fig. 2. It is seen that each space-grid point is represented by three circuit nodes, where the node potentials correspond to the electrostatic potential and the two Fermi potentials associated with the grid point.

The conversion of the semiconductor drift-diffusion equations into an equivalent circuit representation was first proposed by Sah [12], [13], and later pursued by other authors [14], [15]. In this classical transmission-line representation of the one-dimensional semiconductor equations, the equivalent circuit consists of a ladder-like structure of connected nonlinear capacitors and current sources. The electrical coupling

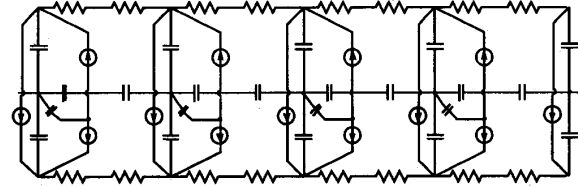


Fig. 3. An example of classical transmission-line representation of the semiconductor equations (after [13]). Note the nonlinear bridging capacitors at every grid node complicating the simulation.

of adjacent grid nodes is accomplished by capacitive current components in the equivalent transmission-line circuit. An example of the classical transmission-line equivalent circuit structure proposed by Sah [13] is shown in Fig. 3. The presence of bridging, nonlinear capacitors between nodes, however, results in a strongly-connected network topology, which may ultimately complicate the numerical solution.

In the modeling approach presented here, in contrast, the local circuit nodes representing grid points are linked through node voltages only. The new formulation approach also eliminates the bridging capacitors and the nonlinear capacitors used in previous circuit element representations. The modularity of the new modeling approach can also be utilized for adjusting the grid point density of the simulated structure [17]. The boundary conditions are established assuming purely ohmic contacts at both external boundaries [10]. The electrostatic potential at the boundary is determined by the externally applied bias voltage, which, in turn, depends on the external load circuit. It is assumed that no voltage drop occurs at the boundary. The conditions for the carrier concentrations at the ohmic boundaries are established by increasing the surface recombination rate. This is accomplished by gradually reducing the electron and hole lifetimes in the Shockley–Read–Hall recombination term by three orders of magnitude for the grid points in the immediate neighborhood of the boundaries.

The calculation of currents is also carried out using the equivalent circuit representation. The total conduction current component across the device is found as the sum of electron and hole currents  $J_n$  and  $J_p$ .

$$J_c = J_n(x_j) + J_p(x_j). \quad (22)$$

The displacement current component is calculated as

$$J_d = -\frac{1}{A} C_{junct} \frac{d}{dt} V_{space-charge} \quad (23)$$

where  $C_{junct}$  represents the junction capacitance, and the space-charge voltage is found by integrating the local carrier densities. The displacement current component for given grid node can be computed directly by taking the time derivative

$$\frac{\partial x_2(j)}{\partial t} = f_2[x_1(j), x_1(j+1), x_1(j-1), x_2(j), x_2(j+1), x_2(j-1), x_3(j), G(j), V_p(j), V_n(j), V_n(j-1), V_n(j+1)] \quad (20)$$

$$\frac{\partial x_3(j)}{\partial t} = f_3[x_1(j), x_1(j+1), x_1(j-1), x_3(j), x_3(j+1), x_3(j-1), x_2(j), G(j), V_n(j), V_p(j), V_p(j-1), V_p(j+1)]. \quad (21)$$

of the local electric field.

$$J_d = -\epsilon \frac{d}{dt} E \quad (24)$$

where  $\epsilon$  is the dielectric permittivity. In the presented model, electrical field is obtained by the difference of the electrostatic potential in the neighboring nodes and time derivation is implemented by a simple circuit involving a voltage source and a capacitor. At every time step, therefore, we readily have all the current components and the total current.

Alternatively, the displacement current can also be evaluated by integrating the time derivative of carrier concentrations in the depletion region.

$$J_d = \frac{C_{junct} q}{\epsilon A} \int_0^{x_m} dy \int_0^y \left[ \frac{\partial p(x,t)}{\partial t} - \frac{\partial n(x,t)}{\partial t} \right] dx. \quad (25)$$

This formulation is particularly useful when the transient variation of electrostatic potential is difficult to evaluate. In the present model, we utilize direct calculation of the drift current at a given grid node using (24).

Given the device structure, grid spacing and the relevant model parameters, the equivalent circuit representation of the semiconductor drift-diffusion equations can thus be readily generated. A conventional circuit simulation program is then used to solve these equations in time domain and to obtain the variation of the electrostatic potential and the Fermi potentials at each grid point. As such, the approach proposed here also makes full use of the numerical stability and efficiency of the well-established circuit simulation routines.

The exponential terms which appear in the space-discretized Poisson's equation (14), and the electron and hole continuity equations (15) and (16) essentially possess the same characteristics as the compact diode model or the BJT Ebers-Moll model equations, which are handled quite well numerically in most conventional circuit simulators. The Bernoulli equation appearing in (15) and (16), which has the general form

$$f(x) = \frac{x}{\exp(x) - 1}, \quad (26)$$

presents a challenge in numerical evaluation for very small values of  $x$ , which is encountered in neutral regions, because the numerator and the denominator approach zero in this case. However, since the function does not possess a singularity at  $x = 0$ , the problem can easily be circumvented by assigning the function its known limit value,  $f(0) = 1$ , for  $x$  values smaller than a certain lower boundary [17]. The availability of absolute value function for nonlinear controlled sources in SPICE provides the alternative option in which (26) is modified as

$$f(x) = \frac{|x| + \delta}{|\exp(x) - 1| + \delta} \quad (27)$$

where  $\delta$  is a small positive number. The value of  $\delta$  (typically  $10^{-6} - 10^{-8}$ ) can be arbitrarily set to control the precision of the equations. A more detailed numerical error analysis is not presented here mainly because the error analysis results derived for conventional circuit simulation tools can be applied directly in this case.

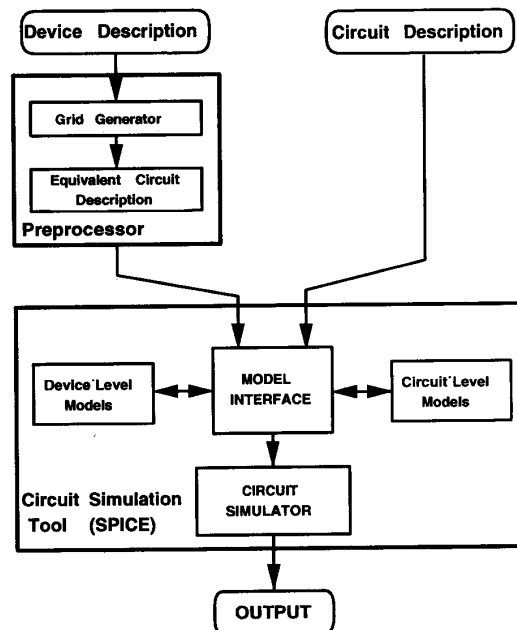


Fig. 4. The proposed mixed-mode device/circuit simulation environment. No additional software tools are required for integration of device and circuit simulation environments.

The simple equivalent circuit representation allows detailed modeling of the internal device structure by locally specifying the physical device parameters. This model allows the investigation of the transient behavior of optoelectronic devices using the local photo-generation term  $G_j$  [17], [18].

It was already mentioned that mixed device/circuit simulation capability using the same simulation tool is very desirable for accurate and realistic assessment of novel devices and integrated circuits. Since the external voltage and current conditions of the simulated device are available at any time point  $t$ , and since the discretized semiconductor equations are being solved using circuit simulation routines, the device simulation approach presented here lends itself to mixed-mode simulation of devices and circuits by directly linking device-level and circuit-level models. The device simulation model described above has been implemented and tested successfully in SPICE and two SPICE-like general-purpose circuit simulation programs. Fig. 4 shows the major components of the combined device/circuit simulation environment.

To facilitate initial dc convergence during the simulation of some semiconductor structures, a simple ramping scheme is used. During preliminary studies [17], the entire structure is initially defined as having the same uniform doping density, with zero potential drop across its external terminals. The dc convergence for this uniform structure can be easily achieved, since the local electrostatic potential and the electron and hole densities will be constant and equal at all grid nodes. Next, the local doping densities and the external boundary conditions are gradually changed (ramped) in time domain, until they reach their actual levels intended for the semiconductor structure.

At this point, the system is in steady-state, and the actual excitation can now be applied either as an electrical or optical pulse waveform.

For the implementation in SPICE [19], dc convergence for a  $p$ - $n$  junction can be achieved without any pre-conditioning or ramping, for moderate doping densities and applied bias. Although there is no formula for the maximum allowable values, and they are usually interdependent, typical numbers are in the order of  $10^{17}\text{cm}^{-3}$  and  $50kT$  for doping and applied bias, respectively, for a  $p$ - $n$  junction. In case of failure to achieve dc convergence, ramping of one or more device parameters can be utilized.

It was also found that abrupt changes in electrical or optical excitation waveforms occasionally cause numerical convergence problems during simulation. To avoid such problems, a "precursor" pulse several orders of magnitude smaller than the actual excitation pulse may be applied first. This small excitation ensures that the carrier density levels rise sufficiently above the steady-state levels, so that the subsequent excitation pulse does not cause numerical problems. Since the magnitude of the precursor pulse is very small, it does not influence the transient response of the device in any significant way. We also noted in SPICE that, if the rising edge of the optical pulse has a staircase structure of arbitrarily small time step size, convergence is assured. In this scheme, pulses with very small rise time (sub-ps) can be accurately represented.

#### IV. SIMULATION EXAMPLES

The applications of the proposed device simulation approach will be demonstrated in this section by simulation examples. Demonstration of this model was initially carried out in SPICE-like general-purpose circuit simulation programs [17]. Recently, the model was also implemented in SPICE [19], and we have noted improved capabilities. The examples presented here were repeated in several different simulation environments, the results presented are obtained using SPICE version 3F2.

The first example investigates the drift and diffusion of excess carriers generated by a localized light pulse in an  $n$ -type semiconductor sample. The semiconductor sample has a length of  $L = 2\ \mu\text{m}$  and a doping concentration of  $N_D = 10^{16}\ \text{cm}^{-3}$ . A voltage of  $50\frac{kT}{q}$  is applied across the sample, and a light pulse focused on the mid-point of the sample is used to generate excess carriers (Fig. 5). Note that this arrangement corresponds to the well-known Haynes-Shockley experiment for the measurement of carrier drift mobility in semiconductors. Fig. 5(b) shows the excess hole concentration within the sample as a function of position and time. It is seen that the generated excess carriers diffuse away from the mid-point and recombine, while the concentration peak moves (drifts) toward the negative-biased end of the sample under applied electric field. This example demonstrates that the equivalent circuit models introduced in Section II accurately represent the transient drift and diffusion behavior of carriers in the semiconductor sample.

The next example investigates the drift and diffusion of excess carriers generated by a localized light pulse in a GaAs

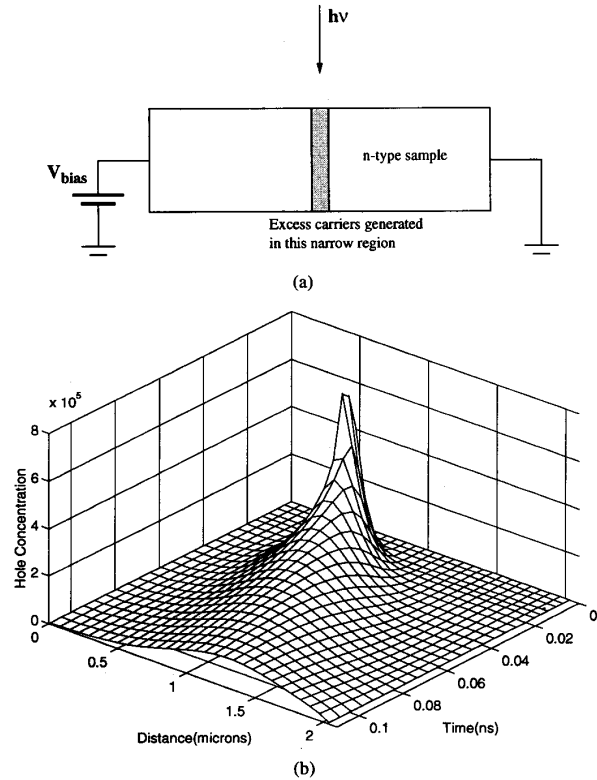


Fig. 5. (a) Uniform  $n$ -type semiconductor sample being subjected to a localized optical pulse excitation, leading to excess carrier generation in a narrow region. (b) Simulated variation of hole concentration as a function of position and time. Generated excess carriers diffuse away from the narrow generation region, while the concentration peak drifts toward the negative-biased end of the sample under applied electric field.

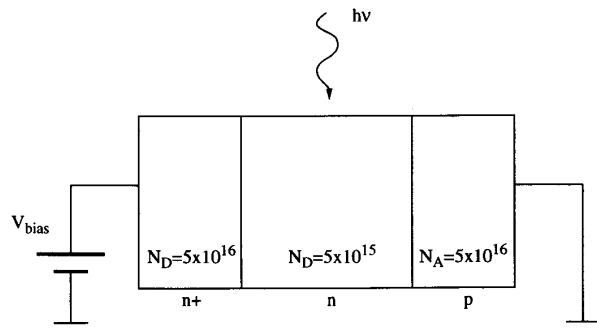


Fig. 6. The simulated GaAs  $p$ - $i$ - $n$  photodiode structure.

$p$ - $i$ - $n$  diode structure (Fig. 6). The total thickness of the device is  $L = 1.5\ \mu\text{m}$  and low doped normally depleted region is  $1\ \mu\text{m}$  thick. A total of 50 grid points were taken with variable spacing, i.e., finer grids at the metallurgical junctions. A small voltage of  $10\frac{kT}{q}$  is applied across the sample to reverse-bias the diode, and a light pulse with 0.1 ps rise- and fall-times and 50 ps duration is focused on the depletion region of the diode.

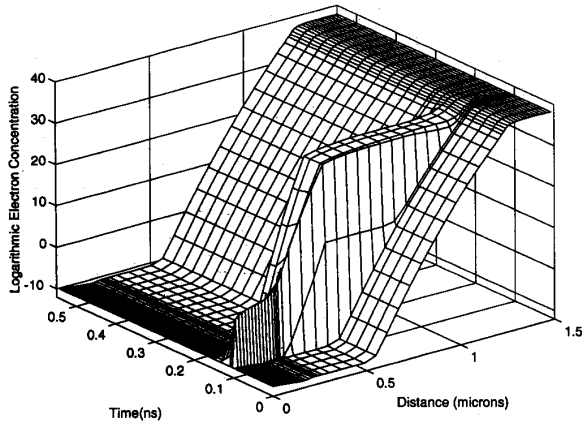


Fig. 7. Simulated variation of electron concentration in a GaAs  $p-i-n$  photodiode as a function of time and position.

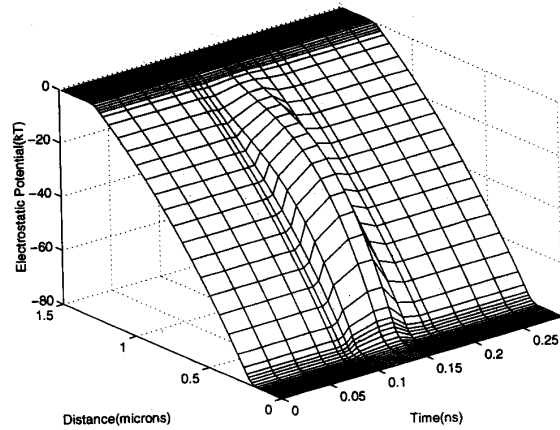


Fig. 9. Simulated variation of electrostatic potential in a GaAs  $p-i-n$  photodiode as a function of time and position.

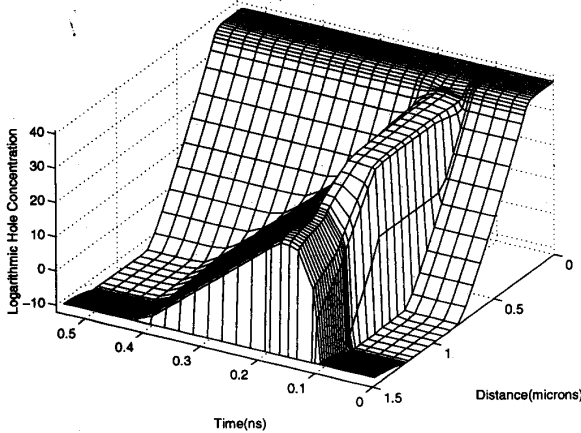


Fig. 8. Simulated variation of hole concentration in a GaAs  $p-i-n$  photodiode as a function of time and position.

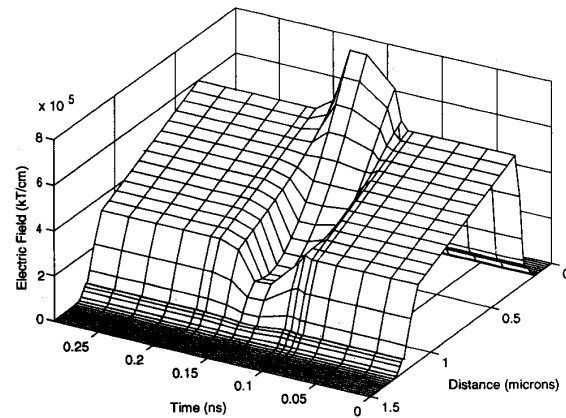


Fig. 10. Variation of electric field in a GaAs  $p-i-n$  photodiode as a function of time and position.

For the demonstration of the concept, uniform optical generation is assumed to take place in the  $0.5\text{-}\mu\text{m}$ -thick region located in the middle of the depletion region. Assuming a 40% quantum efficiency (typical for  $0.5\text{-}\mu\text{m}$  GaAs absorber), the optical excitation corresponds to  $5 \times 10^{21}$  photons/cm<sup>2</sup>·s (i.e., 1 kW/cm<sup>2</sup>). Although the power density seems to be extremely large, the corresponding total power is in the order of 10 mW for a  $30 \times 30 \mu\text{m}$  device, and for the given pulse duration, total energy per pulse is only 50 fJ.

Figs. 7 and 8 show the variation of electron and hole concentrations, respectively, within the sample as a function of position and time. As can be seen from the carrier concentration plots, the optical generation is large enough to create electron-hole densities comparable to those in the neutral regions demonstrating the large signal capability of the presented model. A comparison of transient variation of electron and hole concentrations reveal much smaller transit times of electrons due to higher mobility.

In this example, field dependence of the material parameters were taken into account as dynamic variables. To demonstrate

the importance of transient consideration of material properties, such as mobility, Figs. 9 and 10 show the time and space dependence of the electrostatic potential and electric field, respectively, under the same optical excitation for the photodiode. For the given excitation level, the variation of electric field during the pulse is very prominent. Therefore, the corresponding variation in carrier dynamics, especially in the electron mobility, is very significant. Our model includes an accurate representation of mobility-field dependence for electrons and holes [19].

As described in the previous section, the terminal current for the photodiode is calculated at every time step using dedicated circuits inside the circuit equivalent device model. The photocurrent response of the GaAs  $p-i-n$  photodiode described above is shown in Fig. 11 for two different absorption profiles. The excitation is a 20 ps, 1  $\mu\text{W}$  square pulse. The photocurrent with faster response time corresponds to absorption closer to the p-contact ( $\sim 0.15 \mu\text{m}$  from the depletion edge) resulting in a shorter distance to transit for holes than that for electrons. In this case, the rise and fall times of the current are 8 and

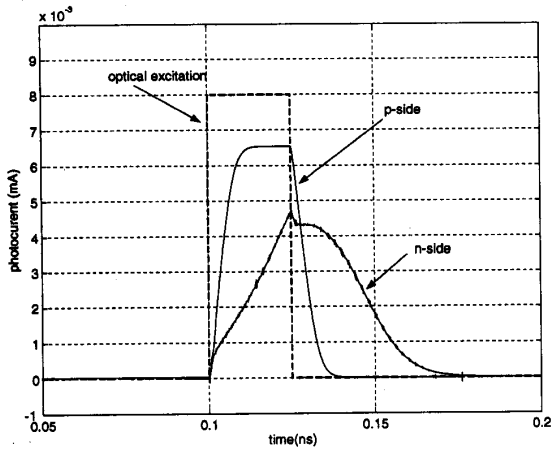


Fig. 11. The current response of the GaAs  $p-i-n$  diode shown in Fig. 6 for two different absorption profiles. The faster response (solid line) corresponds to absorption closer to  $p$ -type contact region, and the slower response is for absorption closer to  $n$ -type contact. Dashed line shows the optical excitation in arbitrary units.

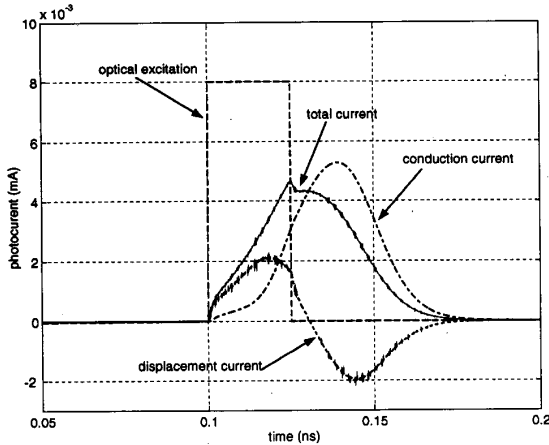


Fig. 12. Detail of the photocurrent displaying transient behavior of displacement (dotted-line) and conduction (dotted-dashed line) components. Dashed line shows the generation term.

9 ps, respectively. Therefore, a photodetector with such an absorption profile will have a flat response up to 50 GHz and a bandwidth approaching 100 GHz. In contrast, for absorption at the opposite end of the depletion region ( $\sim 0.15 \mu\text{m}$  from  $n$ -region) the photocurrent response has a fall time of 40 ps due to the longer transit time of holes.

Fig. 12 shows the conduction and displacement current components for the absorption profile at the  $n$ -side of the depletion region. The delay between the optical pulse and the conduction current is due to long transit time for hole. Besides, a significant fraction of the holes generated in the proximity of the depletion edge diffuse into the neutral  $n$ -region as shown in Fig. 8. For an absorption profile close to  $n$ -region, therefore, the response speed is further limited by the slow diffusion process.

As discussed in Sections II and III simulating optoelectronic devices in a circuit simulator allows for mixed mode

### GaAs $p-i-n$ Photodiode

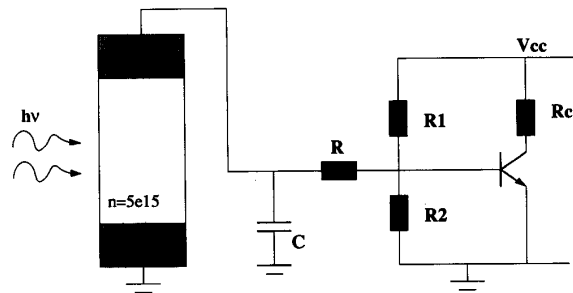


Fig. 13. The simulated photoreceiver circuit composed of a pin diode and a single transistor amplifier. The circuit parameters are  $R_1 = 2 \text{ k}\Omega$ ,  $R_2 = 1 \text{ k}\Omega$ ,  $R_C = 100 \Omega$ ,  $C = 70 \text{ fF}$ , and relevant parameters in the SPICE model for BJT are  $\beta_f = 500$ ,  $I_s = 10^{-14} \text{ A}$ ,  $C_{je} = 30 \text{ fF}$ ,  $C_{jc} = 30 \text{ fF}$ ,  $C_{js} = 20 \text{ fF}$ ,  $r_c = 10 \Omega$ ,  $r_b = 50 \Omega$ , and  $\tau_f = 0.01 \text{ ns}$ .

device/circuit simulation. This capability is demonstrated with the following example of a simple photoreceiver circuit consisting of a GaAs  $p-i-n$  photodiode and a single transistor BJT amplifier circuit (Fig. 13). The supply voltage  $V_{cc}$  is 2.5 V and the bias circuit is adjusted to reverse bias the photodiode and saturate the BJT. In this example, the detailed device level model of the photodiode is combined with the circuit-level lumped models for the rest of the photoreceiver circuit. Since the device-level simulation of the  $p-i-n$  photodiode is carried out using the circuit simulator, the link between the device- and circuit-level simulation results is automatically established. The time-dependent carrier concentrations and the local potential yields the terminal current of the simulated device. The transient current-voltage characteristics of the photodiode is combined with the external circuit, and the voltage boundary conditions are evaluated at every time point by solving the entire OEIC self-consistently. This self consistent solution yields the true large signal response of the device and the OEIC. Fig. 14 shows the simulated photocurrent of the photodetector and the variation of the detector bias under a 50 ps pulse when approximately 0.5 mW is absorbed in the middle of the depletion region.

Fig. 15 shows the transient variation of the base current and collector voltage of the transistor in the photoreceiver circuit. Note that all the circuit variables are evaluated simultaneously with the local device variables. Therefore, the device performance can be tested in realistic bias conditions. Besides, this mixed-mode device/circuit simulation capability enables the circuit designer to easily and accurately investigate the effects of various subtle changes in device geometry and/or material parameters upon circuit performance, while this task would be difficult or impossible using circuit-level device models only.

### V. CONCLUSION

In this paper, a novel approach has been presented for incorporating the transient solution of one-dimensional semiconductor drift-diffusion equations within a general circuit simulation environment. This approach allows simple representation of localized carrier transport models of simulated



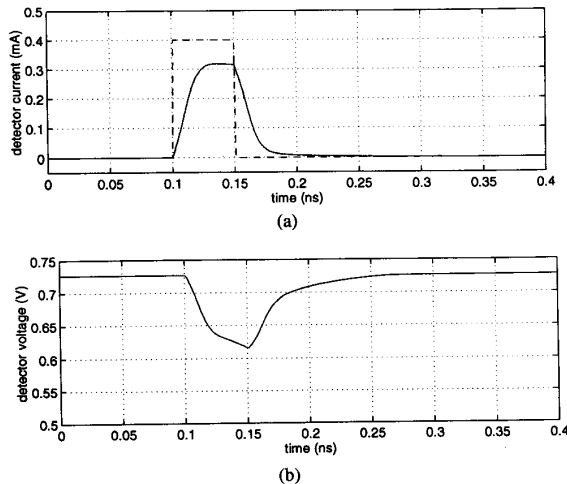


Fig. 14. The transient response of the photoreceiver circuit obtained by mixed-mode device/circuit simulation. (a) Diode current (solid line) and photogeneration (dashed line, in arbitrary units). (b) Transient variation of the photodiode terminal potential.

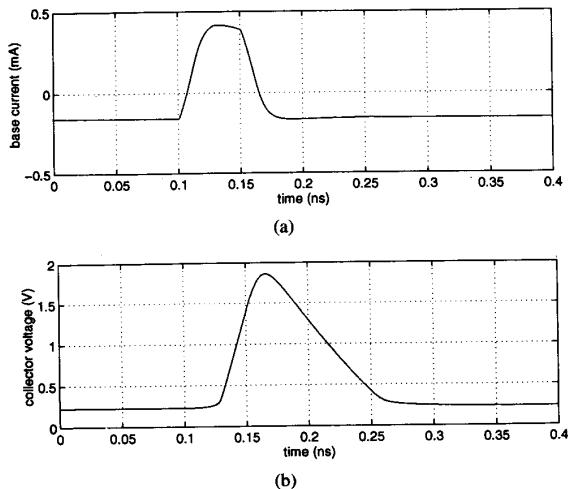


Fig. 15. The transient response of the photoreceiver circuit obtained by mixed-mode device/circuit simulation. Transient variation of base current (a) shows the reversal of bias current under optical pulse. The variation of the collector potential from saturation to nearly to the supply voltage demonstrates the large signal capability of the model.

devices through equivalent circuit elements such as voltage controlled current sources and capacitors. The availability of local photo-generation models at every grid point enables simple simulation of various optoelectronic devices. As the device-level simulation is carried out by the circuit simulator using an equivalent circuit representation, this approach also lends itself to mixed-mode simulation of devices and circuits, by a single simulation tool. The mixed-mode simulation capability of the new approach has been tested for the time-domain analysis of a photoreceiver circuit. It has been shown that the transient characteristics of one-dimensional device structures operating within a realistic circuit environment

can be simulated without requiring dedicated software tools. The device-level modeling approach introduced in Sections II and III can easily be extended for mixed two-dimensional device and circuit simulation. The device simulation model presented in this paper has been implemented and tested in SPICE version 3F2 and also two SPICE-like general-purpose circuit simulation programs. The implementation of the model requires no modifications within the internal structure of the circuit simulator. Thus, it can be implemented quickly and easily on a number of different computation platforms. The versatility of the circuit equivalent representation of the device equations should enable the incorporation of additional differential equations describing other physical phenomena.

## REFERENCES

- [1] M. R. Pinto, C. S. Rafferty, and R. W. Dutton, "PISCES-II - Poisson and continuity equation solver," Stanford Univ., Stanford Electronics Lab. Tech. Rep., Sept. 1984.
- [2] S. Selberherr, W. Fichtner, and H. W. Poetzel, "MINIMOS—A two dimensional MOS transistor analyzer," *IEEE Trans. Electron Dev.*, vol. ED-27, pp. 1540–1550, 1980.
- [3] E. M. Buturla, P. E. Cottrell, B. M. Grossman, and K. A. Salsburg, "Finite element analysis of semiconductor devices: The FIELDAY program," *IBM J. Res. Dev.*, vol. 25, pp. 218–231, 1981.
- [4] M. Reihelt *et al.*, "Waveform relaxation for transient simulation of two-dimensional MOS devices," in *Proc. IEEE 1989 Int. Conf. Computer-Aided Design*, Nov. 1989, pp. 412–415.
- [5] K. Marayam *et al.*, "CODECS: A mixed-level device and circuit simulator," in *Proc. IEEE 1988 Int. Conf. Computer-Aided Design*, Nov. 1988, pp. 112–115.
- [6] W. L. Engl *et al.*, "MEDUSA—A simulator for modular circuits," *IEEE Trans. Computer-Aided Design*, vol. CAD-1, pp. 85–93, 1982.
- [7] G. Chin, Z. Yu, and R. W. Dutton, "A tool toward integration of IC process, device and circuit simulation," in *Proc. IEEE 1991 Custom Integrated Circ. Conf.*, May 1991, pp. 23.6.1–23.6.4.
- [8] K. R. Green and J. G. Fossum, "A pragmatic approach to integrated process/device/circuit simulation for IC technology development," in *Proc. IEEE 1991 Custom Integrated Circ. Conf.*, May 1991, pp. 23.7.1–23.7.4.
- [9] D. L. Scharfetter and H. K. Gummel, "Large-signal analysis of a silicon Read diode oscillator," *IEEE Trans. Electron Dev.*, vol. ED-16, pp. 64–77, Jan. 1969.
- [10] S. Selberherr, *Analysis and Simulation of Semiconductor Devices*. New York: Springer-Verlag, 1984.
- [11] R. F. Pierret, *Advanced Semiconductor Fundamentals*. Reading, MA: Addison-Wesley, 1987.
- [12] C. T. Sah, "Equivalent circuit models in semiconductor transport for thermal, optical, Auger-impact and tunneling recombination-generation-trapping process," *Physica Status Solidi*, vol. 7a, p. 541, 1971.
- [13] ———, "New integral representations of circuit models and elements for the circuit technique for semiconductor device analysis," *Solid-State Electron.*, vol. 30, pp. 1277–1281, Nov. 1987.
- [14] P. C. H. Chan and C. T. Sah, "Exact equivalent circuit model for steady-state characterization of semiconductor devices with multiple energy-level recombination centers," *IEEE Trans. Electron Dev.*, vol. ED-26, pp. 924–936, June 1979.
- [15] K. Kani, "A survey of semiconductor device analysis in Japan," in *Proc. NASECODE 1 Conf.*, June 1979, pp. 104–119.
- [16] M. S. Lundstrom, S. Datta, *et al.*, "Physics and modeling of heterostructure semiconductor devices," Purdue Univ., Tech. Rep. TR-EE 84-35, Sept. 1984.
- [17] Y. Leblebici, M. S. Ünlü, H. Morkoç, and S. M. Kang, "One-dimensional transient device simulation using a direct method circuit simulator," in *Proc. 1992 IEEE Int. Symp. Circ. Syst.*, May 1992, pp. 895–898.
- [18] M. S. Ünlü, Y. Leblebici, S. M. Kang, and H. Morkoç, "Transient simulation of resonant cavity enhanced heterojunction photodiodes," *IEEE Photon. Technol. Lett.*, vol. 4, pp. 1366–1369, Dec. 1992.
- [19] M. S. Ünlü, Bora Onat, and Y. Leblebici, "Large-signal transient simulation of optoelectronic devices," in *Proc. Int. Semiconductor Device Res. Symp.*, Charlottesville, VA, Dec. 1–3, 1993.

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