

Si as a diffusion barrier for Ge/GaAs heterojunctions

S. Strite, M. S. Ünlü, K. Adomi, and H. Morkoç

Materials Research Laboratory and Coordinated Science Laboratory, 1101 West Springfield Avenue, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801

(Received 2 November 1989; accepted for publication 8 February 1990)

We compare the electrical characteristics, before and after annealing, of *p*-Ge/*N*-GaAs heterojunction diodes to similar diodes which incorporate a nominally 10 Å layer of pseudomorphic Si at the Ge/GaAs interface. Both types of diodes exhibit excellent current-voltage characteristics before annealing. Diodes having no Si interlayer show significant degradation after a 20 min anneal at 640 °C. Diodes incorporating the Si interlayer retain excellent diode characteristics after a 20 min anneal at temperatures as high as 720 °C.

Ge is a semiconductor with great potential towards improving existing GaAs- and Si-based device performance. Ge is lattice matched to GaAs, and it has the highest hole mobility-doping product of any device-grade semiconductor. The small band gap and large hole mobility of Ge suggest applications in hole-based modulation-doped structures and phototransistors¹. Further, heavily doped Ge could be used as a low band gap, low resistance base for heterojunction bipolar transistors.²⁻⁴ One major obstacle towards the realization of these devices is cross diffusion at the interface of Ge on GaAs (Ge/GaAs) heterojunctions.⁵⁻⁸

We have previously reported *p*-Ge/*N*-GaAs diodes with nearly ideal electrical characteristics from room temperature down to 77 K.^{9,10} However, for useful device applications, the heterojunction must be able to withstand processing steps and perform over extended periods of time without any degradation, often at elevated temperatures. Annealing is a useful procedure for dopant activation and defect reduction, and it also provides an estimate of long-term heterojunction reliability. In this letter, we report significant degradation in *p*-Ge/*N*-GaAs diode characteristics as a result of annealing. We then repeated the procedure for similar diodes which had an additional 10 Å of pseudomorphic Si at the interface. Diodes with a Si interlayer withstand annealing temperatures as high as 720 °C for 10 min and actually show an improvement in their forward bias current-voltage (*I*-*V*) characteristics with increasing temperature.

The GaAs growth was done by a Perkin-Elmer 430 molecular beam epitaxy (MBE) system. Si deposition took place in an identical but separate MBE system to minimize

contamination from the As background. Ge was deposited in a third vacuum chamber. Samples remained under vacuum during the several minutes of growth interruption required to transfer samples between chambers. All sources were solid source effusion cells.

The diode structures investigated are given in Fig. 1. After GaAs growth, on one sample, nominally 10 Å of Si was grown at a substrate temperature of 500 °C over 1 h at a background pressure of 1×10^{-10} Torr. The other sample was transferred directly to the Ge deposition chamber. On each, 500 Å of Ge was then grown at 60 Å per hour at a substrate temperature at 350 °C. Ge growth was interrupted every 100 Å for Ga delta doping to an estimated hole concentration of $p \approx 5 \times 10^{18} \text{ cm}^{-3}$.

After growth, diodes with various mesa sizes were fabricated by standard photolithographic and wet etching techniques. Diode performance was observed to be independent of device size indicative of a negligible surface recombination current component. Annealing was performed under flowing hydrogen. Nomarski microscope photographs revealed no noticeable change in the surface morphology after annealing. The *n*-type contacts on GaAs were formed by evaporating AuGe/Ni/Au and alloying at 450 °C. Chemical palladium plating was employed for the *p*-type Ge contacts. Both *n*- and *p*-type contacts were verified to be ohmic.

Figure 2 and Table I compare the *I*-*V* characteristics of

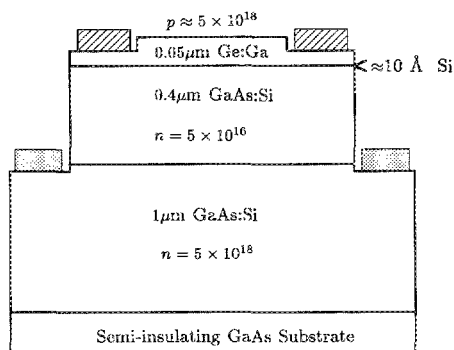


FIG. 1. Device structure of diodes.

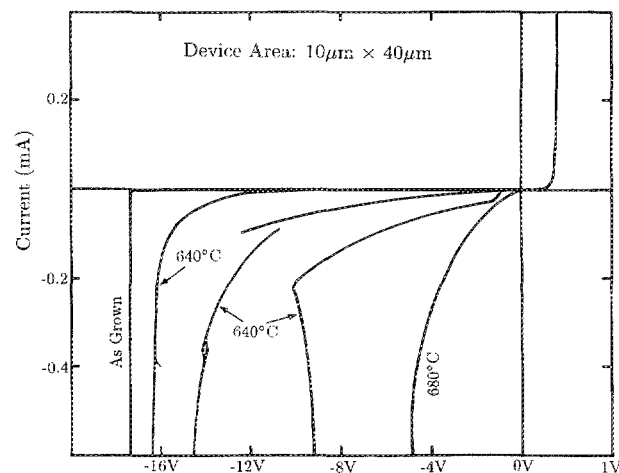


FIG. 2. *I*-*V* characteristics of as-grown Ge/GaAs diodes compared to identical diodes annealed at 640 and 680 °C for 20 min in flowing hydrogen.

TABLE I. Ge/GaAs diode.

Annealing temp. (°C)	Ideality factor n	Saturation current (A/cm ²)
As-grown	1.04	1.5×10^{-7}
640	1.40	$(4.0-8.0) \times 10^{-4}$
680	1.40	$(0.9-1.8) \times 10^{-3}$

Ge/GaAs $p-n$ diodes to identical diodes which have been annealed for 20 min at 640 and 680 °C. The as-grown diodes exhibit the excellent characteristics which we are accustomed to obtaining for the Ge/GaAs system.^{4,9} Devices which were annealed at 640 °C for 20 min showed varied amounts of degradation. Typical devices fall somewhere in between the $I-V$ characteristics shown in Fig. 2. In most of the devices we observed a sharp breakdown at voltages ranging from 9.0 to 16 V which exhibited the oscillatory behavior of microplasma-assisted breakdown.¹⁰ Microplasma-assisted breakdown results from poor sample uniformity, in this case most likely from vacancies in the GaAs as a result of Ga and As outdiffusion into the Ge. Diodes which were annealed at 680 °C all showed significant degradation.

Figure 3 and Table II give typical $I-V$ characteristics for similar diodes which incorporate a nominally 10 Å Si interlayer. The as-grown devices still have excellent diode characteristics and are comparable to the as-grown devices without a Si interlayer. No degradation is observed in samples which were annealed at 680 °C for 10 min and 720 °C for 20 min aside from a decrease in the reverse breakdown voltage, and the forward characteristics actually improved with higher temperatures. Only when we anneal a sample at 800 °C for 20 min do we see a degradation in the reverse characteristics. However, the forward characteristics after the 800 °C anneal are the best observed for any of the diodes studied.

In the devices which did not have the 10 Å of Si, our data support diffusion as opposed to defect generation as the mechanism of degradation. When comparing the as-grown samples, the devices without the Si diffusion barriers have

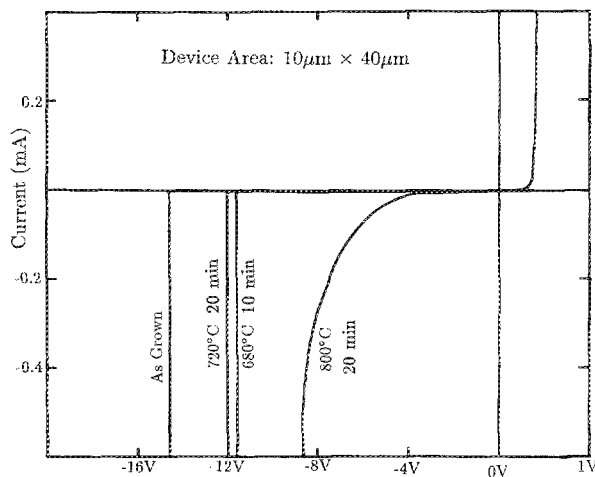


FIG. 3. $I-V$ characteristics of as-grown Ge/GaAs diodes with Si interlayers compared to identical diodes annealed for 10 min at 680 °C and 20 min at 720 and 800 °C.

TABLE II. Ge/GaAs diode with Si diffusion barrier.

Annealing temp. (°C)	Ideality factor n	Saturation current (A/cm ²)
As-grown	1.10	3.7×10^{-8}
680	1.06	2.5×10^{-8}
720	1.05	1.2×10^{-8}
800	1.01	6.4×10^{-9}

slightly superior reverse breakdown voltages and ideality factors, but the saturation current is nearly an order of magnitude higher. The value of the saturation current is strongly dependent on the dopant concentration on each side of the heterojunction. The large saturation current in the devices without the Si interlayer reflects the doping effect of cross diffusion at the interface. As the annealing temperature is raised, the reverse characteristics become increasingly leaky and the breakdown becomes soft. Under forward bias, the ideality factors remain close to unity, indicating the continued predominance of thermionic/diffusion current as opposed to defect-assisted tunneling current. However, the saturation current increases by four orders of magnitude as doping near the interface due to cross diffusion becomes increasingly severe. Further, if defects were being generated, the diodes with the Si interlayer should be similarly affected by the annealing procedure.

The layers which incorporated a Si diffusion barrier maintained excellent reverse characteristics up to 720 °C, while forward characteristics continued to improve up to 800 °C. We attribute the improvement in the forward characteristics to defect reduction as a result of the annealing. At 800 °C, the Si diffusion barrier still restricts cross doping, as seen in the continued reduction of the saturation current, yet the reverse characteristics become leaky and the breakdown soft. The decrease in the reverse breakdown voltage with annealing temperature is likely to be a result of Si diffusion from the heavily doped region beneath the n^- region. This would decrease the reverse breakdown voltage by reducing the GaAs depletion width. If the diffusion is not too severe and does not reach the GaAs in the vicinity of the heterojunction, the forward characteristics should be unaffected. The leakiness of the reverse characteristics after the 800 °C anneal cannot be explained by Si diffusion since the saturation current would be expected to increase. It is possible that the GaAs begins to deteriorate in places at such high temperatures, which would result in the observed nonuniform junction with soft reverse characteristics.

In summary, we compare the performance of Ge/GaAs diodes under various annealing conditions to similar diodes which incorporate a nominally 10 Å Si layer at the interface. Both sets of as-grown devices exhibit excellent diode characteristics. However, while Ge/GaAs diodes show significant degradation after a 20 min anneal at 640 °C, diodes with the Si diffusion barrier retain excellent $I-V$ characteristics even after a 20 min anneal at 720 °C. We conclude that the insertion of several monolayers of Si at the GaAs/Ge interface makes the heterojunction more resistant to cross diffusion at elevated temperatures.

This research is supported by the Air Force Office of Scientific Research (grant No. AFOSR-89-0239) and by the SDIO IST Office through ONR (grant No. N00014-86-K-0513). The authors would like to thank B. Bowdish for technical assistance and C. Litton, K. Evans, and Perkin-Elmer for the loan of equipment which made this research possible. We also thank Professor G.-B. Gao for many useful discussions during the course of this work. One of us (S. S.) wishes to acknowledge the support of NSF graduate fellowship.

¹N. Chand, J. Kiem, and H. Morkoç, *Appl. Phys. Lett.* **48**, 484 (1986).

²Dale K. Judus and Donald L. Feucht, *IEEE Trans. Electron Devices* **ED-**

16, 102 (1969).

³T. Kimura, M. Kawanaka, and J. Sone, *IEEE 47th Device Research Conference*, Cambridge, MA 19-21 June 1989, paper II-A.

⁴M. S. Ünlü, S. Strite, G.-B. Gao, K. Adomi, and H. Morkoç, *Appl. Phys. Lett.* **56**, 842 (1990).

⁵W. Mönch and H. Gant, *J. Vac. Sci. Technol.* **17**, 1094 (1980).

⁶R. A. Stall, C. E. C. Wood, K. Board, N. Dandekar, L. F. Eastman, and J. Devlin, *J. Appl. Phys.* **52**, 4062 (1981).

⁷Robert S. Bauer and J. C. Mikkelsen, *J. Vac. Sci. Technol.* **21**, 491 (1982).

⁸J. H. Neave, P. K. Larsen, B. A. Joyce, J. P. Gowers, and J. F. van der Veen, *J. Vac. Sci. Technol. B* **1**, 668 (1983).

⁹M. S. Ünlü, S. Strite, T. Won, K. Adomi, J. Chen, S. Noor Mohammad, D. Biswas, and H. Morkoç, *Electron. Lett.* **25**, 1359 (1989).

¹⁰J. Chen, G.-B. Gao, J.-I. Chyi, and H. Morkoç, *IEEE Trans. Electron Devices* **36**, 2165 (1989).