Characteristics of annealed *p/n* junctions between GaAs and Si (100)

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Electrical characteristics of a GaAs(*p*)/Si(*n*) interface were determined from capacitance-voltage (*C-V*), current-voltage (*I-V*), and secondary ion mass spectroscopy (SIMS) measurements and compared to those on GaAs(*p*) epitaxial layes on GaAs(*n*) substrates. The comparison was made between the junctions as grown and after an anneal at 850 °C for 20 min in 10% forming gas under an As overpressure. For the GaAs/Si junction the ideality factor changed from 2 or larger to 1.5 and the apparent intercept voltage changed from 2.5 to 1.3 V after annealing. For the GaAs homojunction, the intercept voltage increased from 1.1 to 1.3 V. In addition, the excess current in the forward and reverse bias conditions dropped drastically in the heterojunction. No movement of the metallurgical junction was discernible to within the resolution capability of SIMS. The junction properties obtained by annealing suggest an atomic restructuring of the Si(100) interface during growth or annealing. These new results raise the possibility that the GaAs/Si interface can be made into an electrically viable junction and incorporated into active devices.

In recent years a great deal of activity has taken place to obtain good quality GaAs on Si. Wide ranging research results have been reported dealing with the surface structure of Si substrates before growth,[1] favorable step formation during the initial stages of growth, measured by both high-energy electron diffraction[2] and transmission electron microscopy,[3] and Si-As interaction at the surface, determined by photoemission.[4] Also, various improved growth techniques have been reported including the use of As or Ga prelayers on (100) Si prior to growth,[5] two temperature growth schemes to counter the higher Ga surface migration rate on Si as compared to GaAs,[6] and the use of properly oriented substrates for the reduction of dislocations.[7] All of these schemes have led to surprisingly high quality discrete electronic[8] and optical devices, notably lasers[9] (even continuous wave broad area lasers at room temperature),[10] and most important, integration of GaAs devices with Si devices[11] on Si substrates.

Opportunities provided by GaAs on Si, however, can be enhanced greatly if the GaAs and Si can be integrated actively in the same device. Obviously, this would require a very high quality junction between two material systems having widely differing parameters, e.g., lattice size, thermal expansion coefficient, and electrically non-neutral interfaces even in intrinsic materials.

To obtain a neutral GaAs-Si interface, Wright *et al.*[12] have proposed and used (211) Si surfaces for the growth of GaAs on Si. If the surface of (100) Si were primitive and the GaAs growth were to take place atomic layer by atomic layer, the electric field thus formed at the heterointerface would be much larger than the dielectric breakdown making this interface useless for any active device application. Preliminary results of Won *et al.*[13] in (100) GaAs(*p*)/Si(*n*) junctions were discouraging. Encouraged by recent results on dislocation reduction at the GaAs/Si interface via annealing,[14] the present investigation on heavily doped *p*-GaAs/*n*-Si junctions, grown by molecular beam epitaxy (MBE) and annealed under As_2 overpressure, was taken. Ideality factors of about 1.5 and reverse leakage currents of about 10^{-3} Å/cm^2 at 5 V are obtained on Si substrates which are comparable to those on GaAs substrates.

The samples were grown by MBE following the procedures reported in Ref. 8. After the deposition of 0.5 μm GaAs ($p = 10^{18}$ cm^{-3}), a cap GaAs layer having a Be concentration of 5×10^{19} cm^{-3} was grown to facilitate the ohmic contact formation. After growth, the test samples were annealed for 20 min at 850 °C following the procedure described in Ref. 15. GaAs mesas of 250 μm diameter were then defined on both the test samples and the unannealed samples by selective etching. Finally, ohmic contacts to the GaAs and Si were formed with a Ti/Au metallization, and *I-V* and *C-V* measurements were performed on the wafer using a probe station. It should be pointed out that the metal contacts on GaAs and Si, both of which are heavily doped, were verified to be ohmic.

As reported earlier,[16] capacitance-voltage measurements performed at 1 MHz on as-grown GaAs on Si displayed intercept voltages (extrapolated to $1/C^2 = 0$) of 1.5–2.5 V (shown in Fig. 1 by curve "*A*") indicating the apparent existence of a lightly doped region at the heterointerface. Although the results on the same wafer were consistent, the variation between wafers was responsible for the spread in the intercept voltage. Note that the As doping level in Si is 2.5×10^{19} cm^{-3} and thus most of the depletion region forms in GaAs, which in turn determines the behavior of the *C-V* data. The control sample, grown on a GaAs(*n*) substrate where the electrical junction is between the substrate and the

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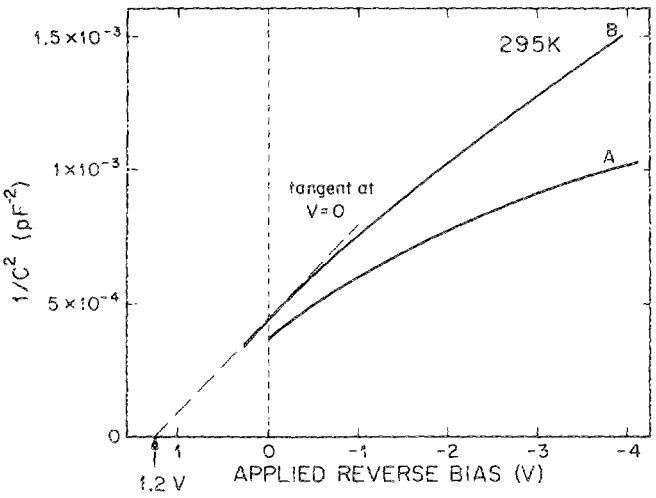

FIG. 1. Capacitance-voltage, plotted as $1/C^2$ vs V, profiles of GaAs on Si p/n junctions before (A) and after 850 °C anneal for 20 min (B).

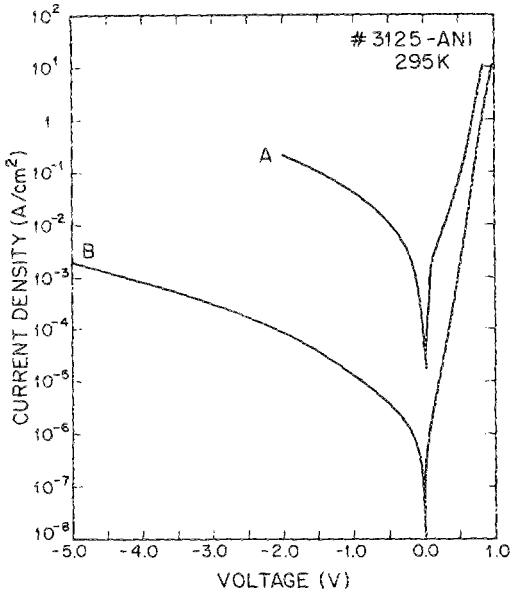

FIG. 2. Current-voltage characteristics of p-GaAs/n-Si (100) junctions before (A) and after annealing (B).

epitaxial layer, exhibited an intercept voltage of 1.1 V indicating the presence of interface charge. These apparent intercept voltages obtained before annealing should be treated with caution since there exists a doping nonuninformity. Together with the results on GaAs substrates, however, these data provide the basis for further study.

After annealing for 20 min at 850 °C, C-V data were taken between $+0.25$ and -4 V. Samples on both GaAs and Si substrates displayed intercept voltages approaching about 1.2 V (shown in Fig. 1 by curve "B"). Furthermore, the variation between Si wafers encouragingly diminished as all the samples revealed intercept voltage values of about 1.2 V. Since the data on GaAs and Si substrates were comparable, only those on Si substrates are shown. An apparent drop in the doping concentration near the junction was noticed in the samples following the 850 °C anneal, which is under further investigation.

The most dramatic effect of annealing manifested itself in the enhancement of the I-V characteristics. Typical forward and reverse I-V curves of a GaAs/Si diode are shown in Fig. 2 before (denoted by an "A") and after annealing (denoted by a "B"). The enhancement of the ideality factor from about 2 to 1.5 for the Si substrate sample is extraordinary. The excess current, which is attributed to defect-assisted tunneling[16] in as-grown samples, is reduced to levels where device considerations may be possible. Similar improvements are also apparent in the reverse bias properties with a three orders of magnitude reduction in leakage current. It should be noted here that the GaAs(p) epilayer grown on GaAs(n) substrate also displayed similar improvements in the reduction of excess current. The reverse current density for 250-μm-diam dots at 5 V is about 10^{-3} A/cm^2 both on GaAs and on Si substrates following the 850 °C, 20 min anneal, which is respectable for doping levels of 10^{18} cm^{-3} on the p side and 2.5×10^{19} cm^{-3} on the n side (Si). The ideality factor of less than 2 is a good indication that the current conduction mechanism is through a combination of diffusion and space-charge currents.

At first glance, the enhanced characteristics observed may possibly have resulted from the outdiffusion of Si, thereby effectively moving the p/n junction into the GaAs epilayer. However, unless this displacement is greater than several hundred angstroms, the diode structure is still dependent upon the heterointerface, and the measured characteristics, comparable to those on GaAs epilayer substrates, demonstrate the respectable quality of the annealed Si-GaAs interface.

To ascertain the position of the p/n junction, secondary ion mass spectroscopy (SIMS) analysis was performed to investigate the behavior of the chemical species before and after annealing. Figure 3 shows the depth distribution of Ga, As, and Si before and after annealing. Within the depth accuracy of the Cameca 3MF SIMS, no change was detected in any of the species in terms of the slopes at the interface or the actual position of the junction. The SIMS results indicate that the (100) interface between GaAs and Si is thermally stable although very localized atomic interchanges cannot be ruled out.

Good I-V and C-V characteristics and chemically stable junctions produced between GaAs and (100) Si are extremely important in terms of the physics of heteroepitaxy. The results reported here suggest a re-examination of the Si-GaAs interface[17] and point to an atomic exchange between Si and possible As (possibly Ga as well). In addition, it is possible that this exchange occurs not only during the deposition of the first interface layer, but continues for the duration of the many monolayer growth.

In conclusion, we have reported that the electrical properties of GaAs (p) on (100) Si (n) junctions enhance considerably after a 20-min anneal at 850 °C under As_2 overpressure. The depth profiles of the constituents Ga, As, and Si, obtained by SIMS, indicate chemically stable junctions with no noticeable junction displacement. These results suggest possible interface reconstruction between Si and GaAs. Achievement of good junction properties be-

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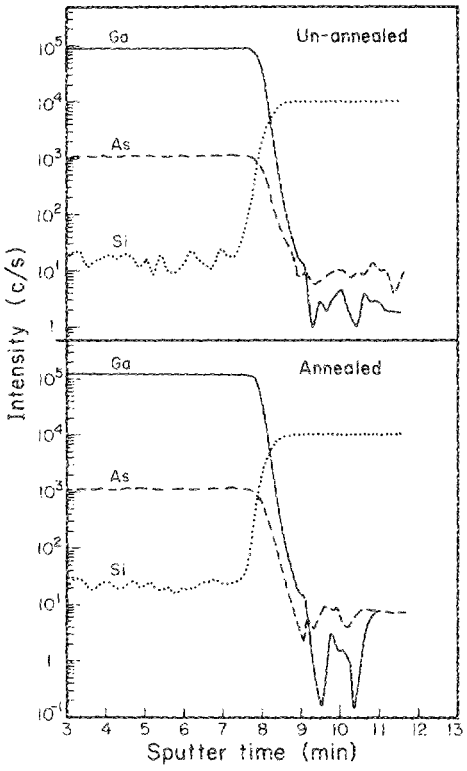

FIG. 3. SIMS profile of *p*-GaAs/*n*-Si heterojunction before and after annealing. Notice the lack of change in the slope of Ga, As, and Si with anneal as well as the lack of junction displacement.

tween Si and GaAs may make possible the use of Si and GaAs collectively in the same device with well-advanced Si device processing technology being available.

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