Uniform junction temperature AlGaAs/GaAs power heterojunction bipolar transistors on silicon substrates

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AlGaAs/GaAs power heterojunction bipolar transistors on Si substrates exhibiting uniform junction temperature distribution are reported. Owing to a unique device design, the temperature spread across the entire device area is about 1 °C. The device exhibits a common emitter current gain of 20, a maximum collector current of 0.6 A, and a collector base junction breakdown voltage of 25 V.

It is well known that heterojunction bipolar transistors (HBTs) fabricated in the AlGaAs/GaAs material system have great potential as high-power microwave amplifiers. Power levels of 2.5 W at *C* band and 2.5 W at *X* band have already been demonstrated in devices on GaAs substrates.[1,2] Power densities of up to 4 W/mm of emitter length in continuous wave (cw) operation have also been reported.[3] GaAs substrates, however, hinder further development because of the low thermal conductivity of this material, about 1/3 of that of Si, which decreases with temperature approximately to the -1.25 power. For Si, the thermal conductivity varies approximately as the -1 power with temperature. Using a three-dimensional (3D) thermal-electrical model[4] and the finite-element method,[5] it has been estimated that the power-handling capability of AlGaAs/GaAs HBTs can be increased by 3.5 and the thermal resistance is reduced by a factor of 2.8 respectively, if Si substrates are used.

Because of a strong positive feedback between the current and junction temperature, it is difficult to make either the junction temperature or the current density distribution uniform for bipolar transistors. For devices in which the active area occupies nearly all of the substrate area, a uniform current distribution leads to a nearly uniform temperature distribution. An example of such devices is the low-frequency Si power transistors for which the measured peak temperature has been shown to increase by over a factor of 3 upon going from a relatively uniform to nonuniform current (temperature) distribution while keeping the total power the same.[6] For HBTs with small lateral dimensions on a large-area substrate, a uniform power density does not lead to a uniform temperature distribution. To achieve a uniform temperature distribution, the power density at the outer edges of the device must be made larger than that in the center. The uniformity of the current distribution in a power HBT can be improved by using a lightly doped layer to form an emitter ballasting resistor.[7]

In this letter, we report theoretical and experimental results describing the effect of emitter ballasting resistor on the junction temperature distribution in power HBTs with multiple emitter fingers. We also present data on junction temperature distribution using AlGaAs/GaAs on Si material system and tapered emitter ballasting resistors.

The power HBT structures investigated were grown in a Perkin–Elmer 430 molecular beam epitaxy (MBE) system on p^- (100) oriented Si substrates. A 0.1 μm undoped GaAs layer was first grown directly on the substrate as the substrate temperature was gradually increased from 460 to 580 °C. A 2.0 μm n^+ subcollector layer, doped 1×10^{19} cm^{-3} with Si, was then grown at a substrate temperature of 580 °C. After that 0.8 μm *n*-GaAs collector layer, doped 1×10^{16} cm^{-3}, was grown, followed by a 0.1 μm GaAs base doped with Be to 1×10^{19} cm^{-3}. Next, a 0.2 $Al_{0.3}Ga_{0.7}As$ emitter doped with Si to 5×10^{17} cm^{-3} was grown at a substrate temperature of 610 °C. A 0.2 μm *n*-GaAs emitter ballasting resistor was then grown, Si doped to 5×10^{15} cm^{-3}, followed by a heavily doped 0.1-μm-thick n^+-GaAs emitter cap layer.

After epitaxial growth, two sets of self-aligned HBTs, one with ten 5×25 μm^2 emitter fingers (HBT_A) and the other with twenty two 6×40 μm^2 emitter fingers (HBT_B), were fabricated by standard wet chemical etching techniques. *n*-type contacts to the emitter and collector layers and *p*-type contact to the base layer were formed by evaporating AuGe/Ni/Au and AuBe, respectively. Polyimide was deposited and etched to the metal contacts, and Ti/Au overlay metal evaporated. The ten emitter fingers of HBT_A possesed equal emitter ballasting resistors. HBT_B consisted of fourteen central fingers with equal ballasting resistors, bounded on each side by four emitter fingers with tapered ballasting resistors, descending from a central resistance value of 2.6 Ω to 1.5 Ω at the device edge.

Typical common-emitter current-voltage characteristics of the power HBT_A and HBT_B are shown in Figs. 1(a) and 1(b), respectively. As can be seen, the current gains on Si substrates are about 20 which are lower than the record gain of 45 obtained in 50×50 μm^2 AlGaAs/GaAs HBT on Si substrate reported earlier,[8] but almost the same as that for unpassivated GaAs on Si devices with 6×6 μm^2 emitters.[9] One can also note the absence of negative differential resistance (NDR) for HBT_B at collector currents below 400 mA and collector-emitter voltage of 8 V. This corresponding power at which NDR first occurs is 3.2 W. In HBT_A this NDR occurs at current levels above 60 mA and

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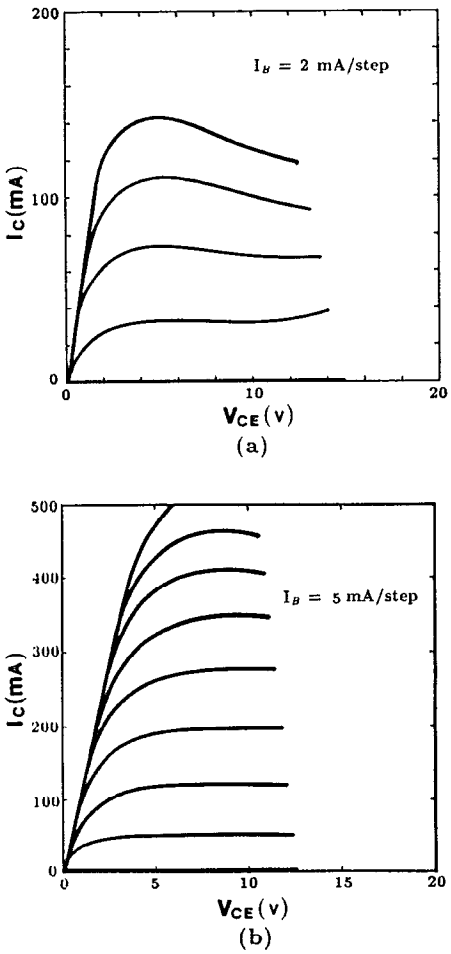

FIG. 1. Typical common-emitter current-voltage characteristics of power HBT_A (a) and power HBT_B (b).

collector-emitter voltage of 6 V. The NDR power is 0.36 W which is only one-ninth the value of HBT_B. If HBT_A had had the same emitter area as HBT_B, the NDR power would at most be 1.5 W. This suggests that the tapered emitter ballasting resistance in HBT_B allows higher current handling capability before any hot spot is formed and self-heating occurs. This is despite the fact that the emitter area of HBT_B is larger than that of HBT_A by a factor of 4.2. This is also confirmed by the dependence of the current gain on current for various collector-emitter voltages and from the surface temperature measurement which will be discussed in detail in the next section.

The maximum available high-frequency current and current gain depend on the falloff rate of the current gain cutoff frequency (f_T) with increasing high current. For HBTs with a high base doping the high level injection in the base is not expected to cause the current gain (h_{FE}) and f_T to falloff; rather the Kirk effect and the junction temperature are responsible for the falloff. Though the falloff rate of both parameters is not quite the same, we can still utilize the falloff of h_{FE} at high currents to monitor the maximum available high-frequency current and define the current at which the current gain drops to one-half of its peak value as the maximum collector current I_{CM}. Figure 2 shows the dependence of the current gain on the collector

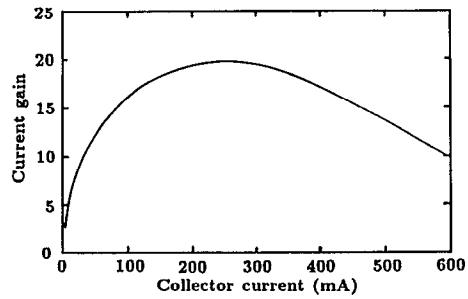

FIG. 2. Dependence of the current gain on the collector current I_C for HBT_B with $V_{CE} = 6$ V and at 300 K.

current I_C for HBT_B at a collector-emitter voltage of 6 V and room temperature. The maximum collector current I_{CM} is 0.6 A corresponding to a current density of 1×10^4 A/cm^2. Collector-base junction breakdown voltage of this device is 25 V.

A power HBT with N emitter fingers having emitter ballasting resistors can be modeled as a parallel combination of N elementary transistors. In the active operating mode, for a given elementary transistor i, the collector current I_{Ci} is given by

$$I_{Ci}=\alpha_{Fi}I_{ESi}\exp\left(\frac{qV_{BE}-R_{Ei}I_{Ei}-R_{Bi}I_{Bi}}{n_ikT_i}\right), \tag{1}$$

Where α_{Fi}, I_{ESi}, R_{Ei}, R_{Bi}, and n_i are the current transfer ratio, the emitter saturation current, the emitter series resistance, the base series resistance, and the ideality factor of the elementary transistor i, respectively.

Since the total collector current I_C is the constant:

$$\sum_{i=1}^{N} I_{Ci}=I_C. \tag{2}$$

The junction temperature T_i of the elementary transistor i relates not only to the self-dissipated power but also to the other elementary transistors, and can be written as[10]

$$T_i=\sum_{j=1}^{N}(I_{Ei}V_{BEi}+I_{Ci}V_{CBi})R_{Tij}+T_c$$

or

$$T_i\cong V_{CE}\sum_{j=1}^{N} I_{Cj}R_{Tij}+T_c, \tag{3}$$

where R_{Tij} is the coupled thermal resistance of the elementary transistor j associated with the elementary transistor i ($R_{Tij} = R_{Tji}$), and T_c is the case temperature. Note that larger R_{Tij} values lead to a rise in junction temperature, meaning larger $T_i - T_c$ values for each elementary transistor i. It is clear that R_{Tii} can be viewed as a self-thermal resistance. When the substrate thickness is larger than the emitter stripe spacing, the coupled thermal resistance R_{Tij} depends sharply on spacing. Therefore, the reduced emitter spacing achieved in self-aligned processes, while reducing the extrinsic capacitance of the device, may increase R_{Tij}.

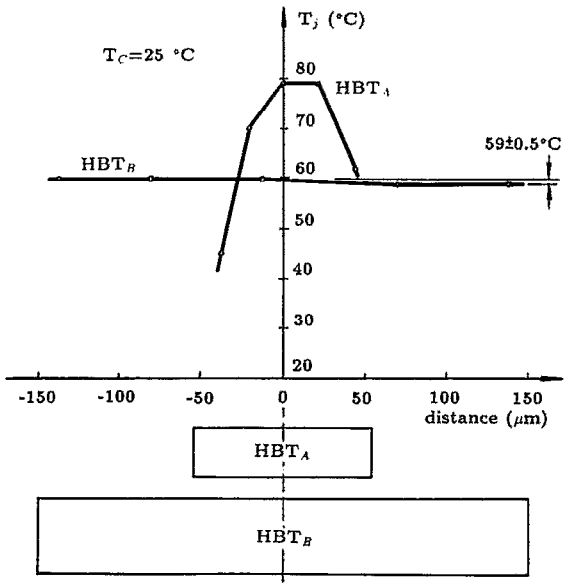

FIG. 3. Surface temperature distribution for HBT$_A$ at 10 V, 100 mA and HBT$_B$ at 10 V, 200 mA measured by infrared microradiometer.

As can be seen from Eqs. (1)–(3), the junction temperature T_j, current I_{Cj}, and emitter ballasting resistance R_{Ei} are three interactive parameters. Meanwhile, T_i, T_j, I_{Ci}, and I_{Cj} $(i \neq j)$ also interact with each other. It is obvious that the emitter ballasting resistor design should be carefully treated as the optimal value is very critical. If R_E is too large, it will degrade the power gain. If R_E is too small, it will not assure a uniform current distribution. As a consequence, the resultant nonuniform current distribution will lead to decreased power gains at high currents.

Using a 3D thermoelectro-feedback model for power HBTs,[4] we designed the tapered emitter ballasting resistor incorporated in HBT$_B$. The resistor values were sufficiently large to lead to a particular current distribution giving uniform junction temperature.

Figure 3 shows the observed surface temperature distribution of HBT$_B$ with 22 emitter fingers and 22 emitter ballasting resistors at V_{CE} = 10 V, I_C = 200 mA, T_c = 25 °C, and HBT$_A$ with ten emitter fingers and ten uniform emitter ballasting resistors at V_{CE} = 10 V, 100 mA, T_c = 25 °C. The temperature measurements were made with a commercial infrared microradiometer. The microradiometer has a spatial resolution of about 15 μm and temperature resolution of about 1.0 °C, and corrects automatically for the emissivity. Due to the limited spatial resolution, the peak value of the surface temperature in the center of HBT$_A$ is actually higher than that measured. However, the spatial and thermal resolutions of the infrared system are certainly adequate for investigating the relative merits of the layout designs of HBT$_A$ and HBT$_B$.

It is found from Fig. 3 that the temperature variation is a mere 1 °C over the entire active region for HBT$_B$ with a corresponding temperature gradient of 3.3 °C/mm. But for HBT$_A$, these values are 28 °C (average) and 280 °C/mm, respectively. Both devices were fabricated on the same wafer grown by MBE on Si substrates. The only difference is the layout design which utilizes the different emitter ballasting resistor arrangement, and in turn leads to the observed junction temperature distributions. From the point of view of device reliability, uniform junction temperature distribution implies a lower peak temperature, which in turn, results in better reliability.

In conclusion, a power HBT with uniform junction temperature distribution has been demonstrated using AlGaAs/GaAs on Si substrates and tapered emitter ballasting resistors.

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