Characteristics of *p*-GaAs/*n*-Si heterojunctions grown by molecular-beam epitaxy

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We have studied the electrical characteristics of *p*-GaAs/*n*-Si heterojunction diodes grown by molecular-beam epitaxy in an effort to investigate the quality of the heterointerface. Both Ga and As prelayers were used to initiate the growth of GaAs epilayers on Si substrates. Current-voltage and capacitance-voltage measurements were made between 300 and 83 K. Ideality factors for heterojunction diodes were as good as $n = 2.0$, despite the 4.1% lattice mismatch between Si and GaAs. At high temperatures the *I-V* characteristics were dominated by generation-recombination mechanisms that lead to a temperature-independent logarithmic slope with applied bias. By removing a thin layer from the Si surface, the surface leakage current was reduced by more than an order of magnitude. The measured intercept voltages, as determined by capacitance-voltage measurements, have no strong dependence on the type of prelayer used to initiate the growth of the GaAs epilayer on Si substrates. The maximum spread in measured intercept voltages was about 1 V, the absolute value of which depends upon the condition of the interface.

I. INTRODUCTION

GaAs on Si has been attracting a great deal of interest because of its potential applications in new hybrid technologies.[1] High-speed devices on Si substrates have been shown to be comparable to those on GaAs substrates.[2,3] However, there are two main difficulties associated with growth of GaAs on Si: lattice mismatch and the formation of antiphase domain (APDs).[4] The former arises because of the unavoidable fact that GaAs has a 4.1% larger lattice constant than that of Si. The latter is due to GaAs being composed of two interpenetrating face-centered-cubic (fcc) sublattices, one for the Ga atoms and the other for the As atoms. Since Si is a nonpolar semiconductor, a uniform Ga or As sublattice is not ensured by the substrate. In order to suppress an antiphase boundary (APBs), i.e., Ga–Ga and/or As–As bonds, the technique of depositing prelayers of Ga or As has been developed.[1]

In a recent letter[5] we reported the shift in intercept voltage obtained from capacitance-voltage measurements for cases of As and Ga prelayers. More recent experiments,[6] however, show that although the intercept voltages obtained range between 1.5 and 2.4 V, there is no direct relation to the type of prelayer. This is more consistent with the established theory[7] and indicates the greatly enhanced sample quality. The shift of intercept voltages observed in Ref. 5 seems to have been caused by the large concentration of defects present in the vicinity of the heterointerface.

The purpose of this paper is to present our much improved results on the electrical characteristics of the heterojunction between GaAs and Si prepared by molecular-beam epitaxy (MBE).

II. EXPERIMENT

The heterojunctions in this study were grown by MBE on As-doped (100) Si substrates (*n*-side) with orientations nominally straight (100), tilted 4° toward (001), and tilted 2° and 4° toward (011). These substrates had nominal resistivities of less than 0.01 Ω cm (measured by the four-point probe method as 0.0034 Ω cm). The epilayer (*p* side) consisted of 0.5 μm of Be-doped GaAs ($p = 10^{18}$ cm^{-3}) and a 0.1-μm cap, which had the doping graded from 10^{18} to 5×10^{19} cm^{-3} to facilitate the formation of ohmic contacts. For comparison, this study also included the growth of a Be-doped GaAs epilayer on Si-doped (*n*-type) GaAs (100) substrate with a nominal resistivity of 0.001 Ω cm ($n = 4.5\times10^{18}$ cm^{-3}).

The preparation of the silicon substrates began with a heavy-metal removal process followed by a series of volatile oxide growth and removal steps. The final step prior to loading into the MBE system consisted of the growth of a protective SiO_2 layer. The details of this procedure are quite similar to the procedure developed by Henderson.[8]

After loading and pumping down the load lock of the MBE system overnight to a base pressure of 2×10^{-9} Torr, the oxide layer was desorbed and surface made primitive by thermally cycling to 1000–1200 °C in an auxiliary chamber. Subsequently, the substrate was immediately transferred to the deposition chamber. After the substrate reached an initial growth temperature of 430–460 °C (as determined by an infrared pyrometer), growth was initiated. An initial exposure of one-half to two monolayers of Ga, As, or simultaneous Ga, As, and Be was used to start growth. The exposure was determined from extrapolated growth curves. For each of the trials, an As cracker was employed to produce As_2 from As_4. Approximately 210 Å of Be-doped GaAs was grown at low temperature and a low growth rate of 1/8 μm/h, after which the substrate temperature and growth rate were increased to 580 °C and 1 μm/h, respectively. The GaAs substrate was prepared by using a standard H_2SO_4:H_2O_2:H_2O etchant, and growth was initiated in a standard manner (i.e., exposure to As flux during outgassing prior to growth).

After growth, GaAs mesas of 250 μm diameter were

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defined by selective etching down to the original Si substrate surface by using a 3:1:50 (NH_4OH:H_2O_2:H_2O) solution. Then Ti/Au metallization was used to make ohmic contacts to the GaAs and Si, as shown in Fig. 1. On these devices we observed very high leakage currents for reverse and small forward biases. This leakage current was reduced by more than an order of magnitude by etching the Si surface in a 1:9:10 (HF:HNO_3:CH_3COOH) solution prior to Ti/Au metallization. Although the etching rate of this solution for GaAs is relatively high, undercutting of GaAs mesas was negligible. The completed device structure is shown in Fig. 1.

III. RESULTS AND DISCUSSION

A. Capacitance-voltage measurements

Capacitance-voltage measurements were carried out in order to investigate the intercept voltage, which is given by[7]

$$V_{\text{int}} = V_0 - \Phi_m - \frac{Q_{\text{is}}^2}{2q(\epsilon_p N_A + \epsilon_n N_D)}, \qquad (1)$$

where V_0 is the true built-in voltage. Q_{is} is the charge per unit area of interface states, and Φ_m represents the dipole term. The dipole effect is produced by the polarization of dangling bonds due to interface states associated with misfit dislocations. A total of more than 20 layers with varying parameters were used in this investigation. Shown in Table I is a list of representative layers from among the many used in this study. Tabulated are the type of prelayer used for each diode and the magnitude of the intercept voltage obtained from extrapolating to forward bias voltages in a plot of $1/C^2$ versus the applied reverse voltage. There are fluctuations in the magnitude of the measured intercept voltages from layer to layer. However, these differences seem to have no direct relation to the type of prelayer used to initiate growth. This is inconsistent with the experimental data of Ref. 5. In view of our present results, we believe that these deviations seem to have been caused by poor interface quality of the previous layers. This analysis is reinforced by the dramatically improved ideality factors shown in Table I. Thus the results of the present study should be considered more reliable.

Figure 2 shows a plot of $1/C^2$ versus applied voltage for each type of diode. The doping profiles obtained from the slopes of these curves are flat, as expected for the uniform doping used in these diodes. Although Fig. 2 shows only one C-V plot for each of the diodes, these curves are representative of many such trials. It must be pointed out, however, that the doping profile in the immediate vicinity of the heterojunction is not accessible through this technique, and it may not be uniform. The intercept voltage varied between 1.5 and 2.4 V over all diodes investigated in this study. The large intercept voltage can be explained by lower doping levels in the vicinity of the heterointerface. Trials of simultaneous Ga and As exposure were also made and the intercept voltage found to be about 1.5 V, which is fairly small compared to those with a Ga or an As prelayer exposure. Since the heterointerface and initial nucleation is extremely complex, more structural and electrical analyses are needed before a widely accepted model is adopted. It appears as though the doping level near the heterojunction is about the same as that intended when simultaneous exposure is used. For a clear understanding of the interface problem, a nearly symmetrically doped ($n = 1.0\times10^{18}$ cm^{-3}) GaAs homojunction was also fabricated (layer No. 7). The C-V measurement gave an intercept voltage of 1.1 V, which is smaller than the calculated value of 1.38 V for the given doping densities. The decrease in the built-in voltage is attributed to the presence of a large number of interface states at the junction according to Eq. (1).

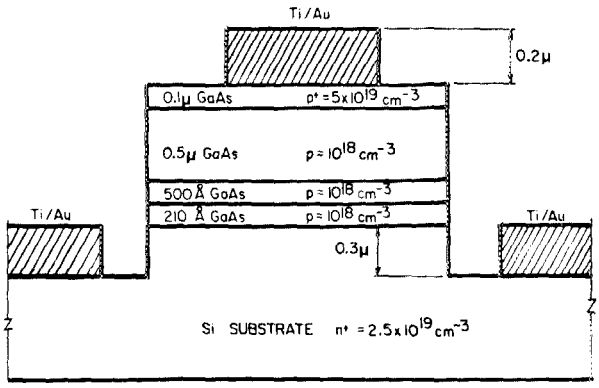

FIG. 1. Schematic cross section of the p-GaAs/n-Si heterojunction diode used in this study.

B. Current-voltage characteristics

Shown in Fig. 3 are the room temperature current-voltage (I-V) characteristics of the p-GaAs/n-Si heterojunction diode with a one-monolayer Ga prelayer (layer No. 3). As can be seen, the diode exhibits sharp turn-on at about 0.7 V and low reverse leakage current with a breakdown voltage of 13 V. It gives an intercept voltage of 2.3 V and ideality factor of $n = 2$, as given in Table I.

Typical room temperature I-V characteristics of the various heterojunction diodes are shown in Fig. 4, and their characteristic parameters are given in Table I. A close examination of Fig. 4 and Table I indicates that the diodes with larger ideality factors have larger leakage currents. As can be seen from Table I, this correlates with longer preexposures. The I-V characteristics of the p-GaAs/n-Si heterojunction diodes are comparable to the homojunction diode.

Shown in Fig. 5 are I-V characteristics with varying temperatures for the heterojunction diode with a one-monolayer Ga preexposure (layer No. 3). As mentioned earlier, about 0.3 μm of the Si substrate was removed from the Si surface in order to reduce the surface leakage current. This etching procedure led to the improvement of the ideality factor and the reduction of the surface leakage current by more than an order of magnitude. In the high-bias region of the curve of Fig. 5, an ideality factor of $n = 2.0$ was obtained at room temperature. Table II shows the ideality factors measured in different voltage ranges for the diode of Fig. 5. Some of the voltage intervals are left blank, because the diodes started to saturate because of the series resistance effect. We observe that the voltage range of the minimum ideality factor shifts to higher-voltage intervals with decreasing tem-

TABLE I. Description of diodes.

Layer No.	Acceptor concentration of GaAs epi (cm^{-3})	Types of prelayers	Tilt orientation	Intercept voltages (V)	Ideality factors
1	1.0×10^{18}	one monolayer As	4°→⟨001⟩	2.2	2.3
2	1.0×10^{18}	one monolayer Ga	4°→⟨001⟩	1.8	2.8
3	1.0×10^{17}	one-half monolayer Ga	4°→⟨001⟩	2.3	2.0
4	1.0×10^{17}	one-half monolayer Ga	4°→⟨001⟩	IND[a]	2.2
5	1.0×10^{17}	one-half monolayer Ga	4°→⟨001⟩	2.0	2.4
6	1.0×10^{17}	SIM[b]	4°→⟨001⟩	1.5	2.3
7	1.0×10^{17}	GAS[c]	GAS	1.1	2.9
8	1.0×10^{18}	one-half monolayer Ga	4°→⟨001⟩	2.2	3.6
9	1.0×10^{18}	two monolayers As	4°→⟨001⟩	1.6	3.5
10	1.0×10^{18}	one-half monolayer Ga	4°→⟨001⟩	2.0	3.2
11	1.0×10^{18}	one-half monolayer Ga	4°→⟨110⟩	2.4	4.3
12	1.0×10^{18}	one-half monolayer Ga	2°→⟨011⟩	1.6	4.5
13	1.0×10^{18}	SIM	⟨100⟩	1.6	5.8

[a] IND, curvature of a plot of $1/C^2$ vs V did not allow accurate extrapolation.
[b] SIM, simultaneous exposure of Ga and As.
[c] GAS, GaAs epilayer on GaAs(100) substrate.

perature. This is due to the fact that the turn-on voltage shifts in a positive manner as the temperature decreases. It also should be pointed out that the ideality factor increases with decreasing temperature, as seen clearly in Table III. Table III also shows the ideality factors and logarithmic slope constants α for low- and high-forward-bias regions.

A quantitative comparison of the current mechanisms in high-bias regions with those in low-bias regions was made by determining first the value of ideality factor and then calculating the logarithmic slope constant (reciprocal of the product of the ideality factor and temperature) at a given temperature. In the high-bias region the ideality factor is about 2 and increases as temperature decreases. This implies recombination effects that can have several different, nonexclusive origins, such as recombination due to deep levels in the depletion layer,[9] surface recombination at the perimeter of the depleted surface,[10] and the interfacial recombination through interface states at the heterojunction.[11] The relative

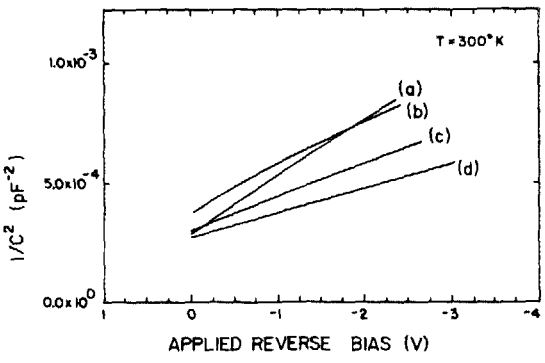

FIG. 2. Plot of $1/C^2$ applied reverse voltage for several diodes at 300 K. (a) No. 7, GaAs homojunction diode; (b) No. 6, P-GaAs/n-Si heterojunction diode with simultaneous preexposure of Ga and As; (c) No. 2, P-GaAs/n-Si heterojunction diode with 5-s Ga preexposure; (d) No. 1, P-GaAs/n-Si heterojunction diode with 5-s As preexposure.

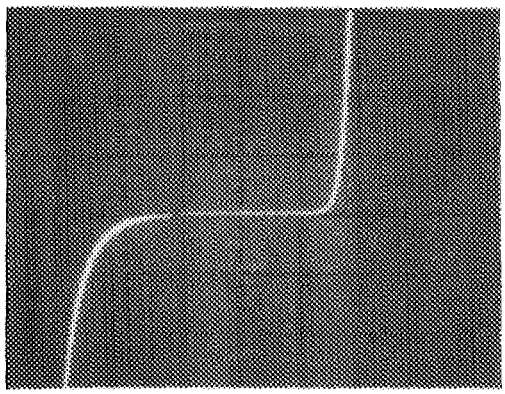

FIG. 3. Curve tracer scan of the current-voltage characteristics of heterojunction diode (vertical, 2 mA/div; horizontal, 0.5 V/div for forward, 5 V/div for reverse characteristics).

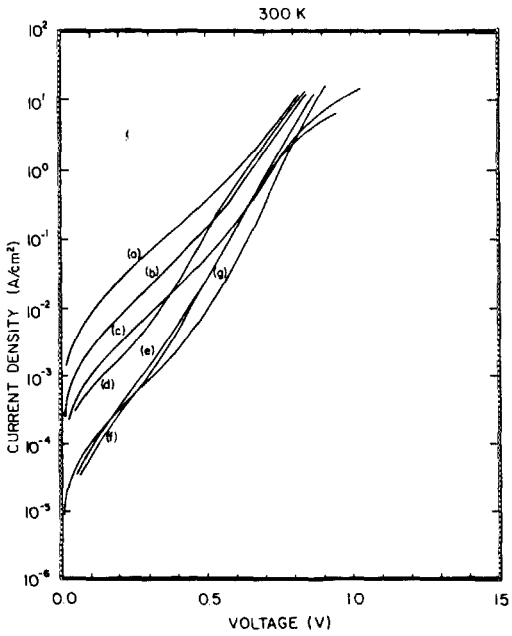

FIG. 4. Semilogarithmic plot of the current-voltage characteristics of the several diodes at room temperature. (a) No. 7, $n = 2.9$; (b) No. 2, $n = 2.8$; (c) No.1, diodes with a Ga prelayer, $n = 2.3$; (d) No. 7, $n = 2.9$; (e) No.1, diodes with a As prelayer, $n = 2.3$; (f) No. 4, $n = 2.2$; (g) No. 3, $n = 2.0$.

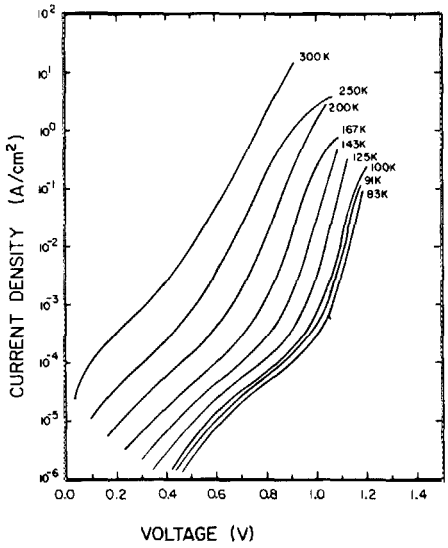

FIG. 5. Semilogarithmic plot of the current characteristics of No. 3 with varying temperature.

contribution of the surface recombination at the junction perimeter of the depleted surface can be investigated by looking at the current characteristics of variable-size diodes. If the I-V characteristics are influenced by the surface recombination at the exposed perimeter of the junctions, the current density should increase linearly with the perimeter-to-area ratio.[10] Circular mesa diodes with diameters from 9 to 100 μm were fabricated, and the logarithm of the measured current densities were plotted against the diameter of the circular mesa. Unfortunately, the data points were so scattered that no accurate correlation between current density and diameter of diodes could be determined. It is, however, likely that the surface recombination at the depleted perimeter does not dominate the current characteristics. As shown in Table III, the logarithmic slope constant α at low temperatures is nearly independent of temperature. This implies that tunneling dominates the I-V characteristics at these temperatures, which is in good agreement with common findings. Figure 6 indicates that the current density of the diodes given in Table I closely follows the relationship given by

$$J = J_0 \exp(\alpha V). \tag{2}$$

To examine the current mechanism in further detail, the ideality factor n and the logarithmic constant α at low forward biases are also given in Table III. A close inspection of the data indicates that the ideality factor increases as the temperature decreases, but the logarithmic slope remains constant over all temperature ranges. This is quite similar to the case of p-(AlGa)As/n-GaAs heterojunction diodes under low forward biases.[12] There are, however, important differences between p-GaAs/n-Si and p-(Al,Ga)As/n-GaAs heterojunction diodes. Since GaAs/Si system is a polar/nonpolar heterojunction, it does have more interface states than the polar/polar (Al,Ga)As/GaAs heterojunction. Therefore, in the GaAs/Si heterojunction diodes, the den-

TABLE II. Ideality factors of diode No. 3 for the different voltage ranges with varying temperature.[a]

Temperature (K)	Voltage ranges (V)					
	0.6–0.7	0.7–0.8	0.8–0.9	0.9–1.0	1.0–1.1	1.1–1.2
300	2.1	2.0	2.3	2.1		
292	2.1	2.1	2.7	2.3		
250	2.3	2.2	2.8	3.0		
200	3.9	2.7	2.3	2.8		
167	6.8	4.5	2.9	2.4		
143	9.8	8.0	4.8	2.8	2.4	
125	11.7	11.0	8.2	4.2	2.5	
100	13.2	14.4	13.3	4.3	3.8	
91	13.4	15.9	15.0	10.0	4.5	3.7
83	14.7	17.4	16.7	12.0	5.9	3.4

[a] At low temperature the current is dominated by $I = I_0 \exp(\alpha V)$, where α is around 25 V^{-1}.

TABLE III. Ideality factors and logarithmic slope constants for several diodes at various temperatures.

	Temperature (K)	High-bias region		Low-bias region	
		n	α	n	α
Layer No. 3	300	2.0	19	2.1	18
	250	2.1	22	2.3	20
	200	2.2	26	2.7	21
	167	2.3	30	2.9	24
	143	2.4	34	2.8	29
	125	2.5	37	4.2	23
	100	3.8	31	4.3	27
	91	3.7	34	4.5	28
	83	3.4	41	5.9	24
Layer No. 1, Ga	300	2.3	17	2.4	16
	250	2.5	19	3.1	15
	200	2.7	21	2.8	21
	167	3.1	22	3.7	19
	143	3.0	27	3.4	24
	125	3.4	27	4.3	22
	100	4.3	27	6.3	18
	91	4.8	27	7.4	17
	83	5.6	25	8.3	17
Layer No. 1, As	300	2.3	17	2.6	15
	250	2.4	19	2.5	19
	200	2.5	23	2.8	21
	167	3.1	22	4.0	17
	143	3.3	25	4.1	20
	125	3.3	28	3.9	24
	100	3.8	31	5.3	22
	91	4.4	29	6.3	20
	83	4.9	29	7.2	19

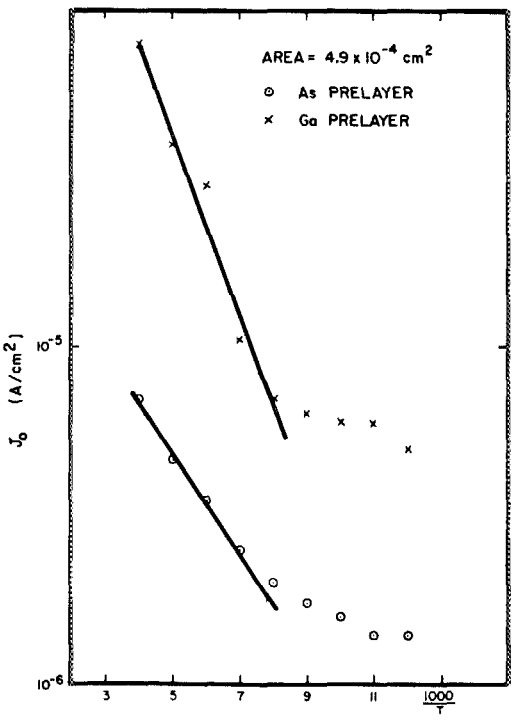

FIG. 6. Temperature dependence of saturation current density J_0, where $J = J_0 \exp(qV/nkT)$ (No. 1).

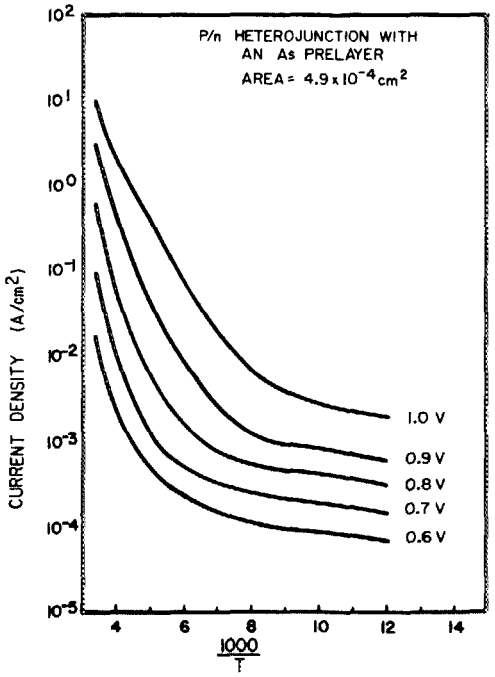

FIG. 7. Semilogarithmic plot of current density vs reciprocal temperature for the diodes with an As prelayer (No. 1).

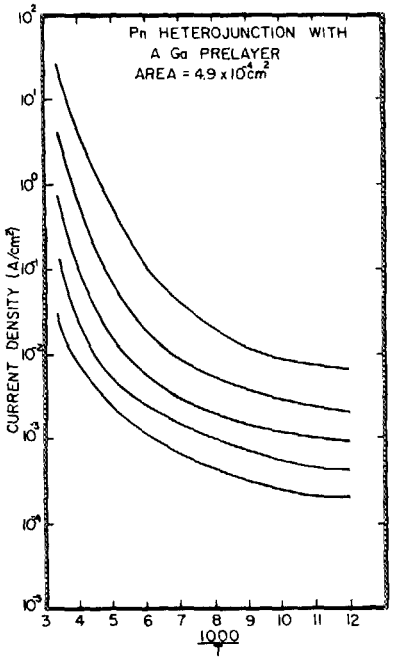

FIG. 8. Semilogarithmic plot of current density vs receiprocal temperature for the diodes with a Ga prelayer (No. 1).

sity of interface states is sufficiently high to produce a large interfacial recombination current.

Etching experiments on layer No. 1 revealed that the growth of GaAs on some regions of the silicon surface was initiated with a Ga prelayer, while in some other regions it is initiated with a As prelayer. This takes place only when about one-half monolayer of As or Ga exposure is used and is found to be due to a difference in temperature across the substrate. This layer enabled us to make an accurate comparison of the electrical characteristics between the diodes with a Ga prelayer and those with an As prelayer. A semilogarithmic plot of the current-density–voltage characterisitics is shown in Figs. 7 and 8 for Ga and As prelayer cases, respectively. Comparison of Figs. 7 and 8 show that the current density of diodes with Ga prelayers is larger than those with As prelayers.

In order to be confident in our electrical findings about the interface properties, we have conducted photoluminescence experiments on several layers. The photoluminescence results from these thin GaAs epilayers grown on Si are one-third to one-half the intensity of those on GaAs substrates. This demonstrates that, despite the lattice mismatch, these GaAs layers grown on Si are of good quality. The details of the photoluminescence results will be reported later.

IV. CONCLUSIONS

We have studied the current-voltage and capacitance-voltage characteristics of P-GaAs/*n*-Si heterojunction diodes between 300 and 83 K temperature range. We have found that the current conduction mechanism obeys the $J = J_0 \exp(qV/2KT)$ relationship at high temperature and the $J = J_0 \exp(\alpha V)$ relationship at lower temperatures with high bias or over all temperature ranges with low forward bias. It was observed that the current conduction mechanism is due to tunneling limited interfacial recombination at lower forward biases. Capacitance-voltage measurements showed that the intercept voltage does not change very much with the type of the prelayer used to initiate the epilayer growth on the Si substrate. This indicates that there is an atomic reconstruction of the GaAs/Si interface. The consistent behavior of the *I-V* and *C-V* measurements were also confirmed by the photoluminescence studies, which indicated that our layers were of good quality.

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